STATES PATENT AND TRADEMARK OFFICE

JOSEPH T. EVANS, JR., ET AL.

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Examiner:

Alvssa H. Bowler

For:

NON-VOLATILE MEMORY CIRCUIT USING

FERROELECTRIC CAPACITOR STORAGE ELEMENT

RECEIVED

Honorable Commissioner of

Patents and Trademarks

JUL 1 1 1991

Washington, D.C. 20231

GROUP 230

Dear Sir:

DECLARATION OF LEO N. CHAPIN

I, Leo N. Chapin, of 1503 Yukon Drive, Sunnyvale, California 94087, do hereby declare that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true, do hereby declare as follows:

I was employed at Krysalis Corporation, Albuquerque, New Mexico, from December 4, 1985, to September 1, 1989, when the assets thereof were purchased by National Semiconductor Corporation of Santa Clara, California.

> t hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Cemmissioner of Patents and Trademarks.

Washington, D.C. 20231 or

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DECLARATION OF LEO N. CHAPIN - Page 1

2. My job title during the years of 1986 and 1987 was Research Associate and my responsibilities were the synthesis of sol-gels and the depositions of all ferroelectric films on substrates.

To the best of my knowledge, the integration of ferroelectric material on silicon to form microelectronic memory circuits was not attempted before, and thus all the processes, techniques and materials had to be developed by Krysalis by experimental and trial and error techniques.

- 3. Among my various responsibilities while employed at Krysalis, I developed and maintained a log of the wafers that I processed with ferroelectric material.
- 4. Exhibit A attached hereto is a copy of a "FES Coating Log" that I developed and maintained while employed at Krysalis. The log illustrates various wafers processed at Krysalis between August 2, 1986, and September 29, 1987.
- 5. The data input into a data base and represented by Exhibit A was carried out by myself while at Krysalis, using a Macintosh personal computer, Model MacPlus, and using a then commercially available program called "Overview". The Overview program is a relational type data base adapted for storing data and presenting the data in desired formats. The FES coating log data was stored on a magnetic three and one-half inch floppy disk during all times, including the present time. I found the computer and software a reliable system for storing and retrieving data for the FES coating log.

- During the course of gathering evidence for this matter, I recalled that I still had the magnetic disk with the FES coating log data. However, I no longer had the "Overview" program, but instead had a commercially available "Panorama" software data base program used on my Macintosh personal computer. The Panorama program was designed by the original makers of the Overview program, but allows data input by the Overview format to be output under the new In printing out the original FES coating log data previously stored on the floppy disk using the Panorama software and the Macintosh personal computer, I inputted column headings for the data to provide the printout of Exhibit A. The actual FES coating log data itself was last changed on the floppy disk November 4, 1987, as indicated at the bottom of each page of the printout of Exhibit A.
- 7. The "Date Coated" column of Exhibit A indicates the day Krysalis processed wafers by depositing thin film ferroelectric material on the virgin or preprocessed wafers.
- 8. The "Film ID" column identifies the particular substrate or semiconductor wafer on which the ferroelectric material was deposited by Krysalis.
- 9. As an example of interpretation of the FES coating log data, on page 9 of the log, semiconductor wafer "6310A" was coated with a ferroelectric material on November 6, 1986.

The other entries in the log associated with the 6310A wafer are identified as follows:

"OrbTD01cmos" under the heading of "Substrate
Description" means that the wafer itself was fabricated by
Orbit Semiconductor. The wafer was a TD01 test wafer (TW)
with CMOS transistor circuits.

"Adeline" was an arbitrary name associated with the "6310A" TD01 wafer as it was processed, tested and evaluated by Krysalis.

Under the column heading "Bel Type", there is noted the different types, if at all, of bottom electrode materials. The question mark for the 6310A CMOS test wafer means that the type of bottom electrode material was unknown to me at the time the data was entered into the log.

After depositing the ferroelectric material, and patterning the material so as to form a capacitor dielectric at various locations on the wafer, the wafer was annealed or sintered at a temperature of 550°C to transform the material into a ferroelectric ceramic that exhibits a hysteresis characteristic.

"G6300" under the column heading "Sol-Gel ID" identifies the date the ferroelectric material was formulated by Krysalis. "G" means a sol-gel type of ferroelectric material. The "6" means 1986, and the "300" means the 300th day of 1986, i.e., October 27, 1986. The term "(8/40/60,+10),10" under the same heading identifies the respective amounts of lanthanum, zirconium and titanium in the PLZT ferroelectric sol-gel material. The "+10" term indicates an atomic percentage of excess lead. The "10" term outside the parenthesis means that a period of ten days passed between the time the ferroelectric sol-gel material itself was formulated and thereafter deposited on the wafer.

The designation "10cts" under the column heading "Coats & Spin, Speed" indicates that ten separate coats or layers of the ferroelectric material were deposited on top of each other to form a composite layer of the ferroelectric dielectric material. The ferroelectric material was spun on the wafer in liquid form at a speed of 2000 rpm.

In the early development efforts at Krysalis, each thin film layer of liquid ferroelectric material was sintered separately for a time period of about forty-five minutes to form a hardened ceramic film. The column heading "Sinter Profile" identifies the sintering temperature. The high temperature sintering effectively converted the film amorphous material into a Perovskite crystalline material that exhibits ferroelectric characteristics. The combined sintering steps themselves often took several hours.

The "Bake Profile" column of the log of Exhibit A has an entry "NA" (not applicable) until about December 17, 1986, at which date the processing of the individual ferroelectric layers was modified. Rather than conducting a high temperature sintering step of each layer, as was previously done, each ferroelectric film layer was baked for a short period of time to drive off organics, and then after the last layer was applied, the entire layered structure was sintered at a higher temperature. For example, the wafer identified with Film ID 6351A on page 10 of the log was processed by baking each layer for two minutes at a temperature of 300°C, i.e., the designation of "2@300" in the "Bake Profile" column of the log. Then, the entire layered ferroelectric material was sintered for thirty minutes at 650°C in an oxygen environment, i.e., the designation of "30@650inO," in the "Sinter Profile" column of the log.

10. It is to be noted in the log of Exhibit A that I processed other CMOS wafers bearing Film IDs including 6315B and 6332A through 6342D on dates between November 13, 1986, and December 8, 1986. These CMOS wafers noted in the log were TD01 test wafers, although not identified in the log as such. The TD01 CMOS test wafers each had many die with CMOS transistor memory circuits fabricated by Orbit

Semiconductor, Inc., and with the transistor circuits connected to ferroelectric capacitors as fabricated at Krysalis. Each die of the TD01 CMOS test wafers had a memory cell arrangement with complementary transistors and ferroelectric capacitors.

11. Other CMOS test wafers processed by Krysalis to completion are identified in the log of Exhibit A as follows:

Date Coated
2/12/87
2/13/87
2/13/87
2/17/87
3/23/87
4/07/87
4/08/87
4/14/87
4/27/87
6/16/87

12. Other test wafers, termed "ECD512" or "512ECD" wafers, were processed by coating and patterning ferroelectric material thereon, starting on April 8, 1987, as indicated by Film IDs 7098E-7100B.

The wafers associated with these Film IDs were silicon wafers that were etched by Orbit Semiconductor, Inc., to form a topography similar to other wafers to be later fabricated with CMOS memory circuits. These initial test wafers were processed through the Krysalis ferroelectric processes as trial runs in preparation for the more expensive ECD512 wafers which had the CMOS memory circuits. As noted in the log, these test wafers were processed with different parameters to determine the results. For example, wafer 7098G had a silicon dioxide layer over which the ferroelectric material was spun. Wafers 7099A-7105B had silicon nitride layers, but some wafers had different types

and layers of bottom electrode materials, processed at different temperatures.

Actual ECD512 wafers with CMOS memory circuits were processed by Krysalis shortly thereafter and are identified in the log as follows:

Film ID	Date Coated
7105C,D	4/15/87
7117B	4/27/87
7125F	5/05/87
7135B,C	5/15/87
7139A	5/19/87
7148A,B	5/28/87
7156A,B	6/05/87
7160A	6/09/87
7162A-D	6/11/87

Like the TD01 CMOS test wafers, the ECD512 CMOS wafers were processed with ferroelectric material layers to form non-volatile memory cells. However, the ECD512 CMOS wafer had many die each with an array of 64x8 memory cells.

13. The ECD512 CMOS wafers were supplied to Krysalis by outside semiconductor vendors who carried out the actual semiconductor processing to form CMOS transistor circuits according to Krysalis specifications. The ECD512 CMOS wafers were subsequently processed by Krysalis personnel, either by myself, or others under my supervision and control, to deposit and pattern the ferroelectric sol-gel material to form a pair of ferroelectric capacitors in association with each memory cell. The patterning of the ferroelectric material to form the individual capacitor dielectric areas on the wafer was carried out using masks that were made by outside vendors according to Krysalis specifications.

- 14. I conducted numerous experiments and tests while at Krysalis with different compositions of ferroelectric materials to determine if they could be deposited and adhered to different types of bottom electrode conductor materials formed on semiconductor wafers, to determine if the ferroelectric material would be compatible with semiconductor wafer processing techniques, and if the ferroelectric material would operate satisfactorily over long periods of time with acceptable levels of fatigue and aging.
- 15. Among the number of Krysalis tests conducted with ferroelectric material, there is shown in the log Film IDs 7030A,B which had a thermal silicon dioxide grown over the surface of the silicon wafer, but with no bottom electrode material. The ferroelectric material was applied to the wafer on January 30, 1987. With respect to wafer 7030B, two different compositions, and thus two different layers of ferroelectric material were applied on the same wafer. coats of one type of ferroelectric material was applied directly over the silicon dioxide surface, with six coats of a different ferroelectric material thereover. believed that tests were conducted to determine if lead would diffuse into the silicon dioxide material during the sintering operation. Also, because the bottom two coats of the ferroelectric material had no zirconium, tests were carried out to determine if the cracking of the ferroelectric material during the sintering operation was alleviated.
- 16. Also on January 30, 1987, wafer 7030D was coated with eight layers of a particular type of ferroelectric material, and the wafer was annealed after the top electrode deposition. The annealing was carried out at about 400°C to

determine if a better bond could be obtained between the top electrode material and the ferroelectrode material.

- 17. During February 4 and 5, 1987, wafer 7035A-7035C and 7036A-7036D were processed with a first bottom layer of ferroelectric material, and seven layers of a different ferroelectric material thereover. It was found that the G6307 ferroelectric material exhibits less cracking during the sintering operation, when deposited over silicon dioxide. Also as noted, the different compositions of ferroelectric material included 8/40/60; 15/0/100; 3/60/40; and 0/50/50. Also, some of the wafers had a bottom electrode, and some had the ferroelectric material deposited directly on the silicon dioxide.
- 18. On February 6, 1987, wafers 7037A, B and C were prepared with composite layers of ferroelectric material on different thicknesses of a spin-on oxide. For example, wafer 7037A had a thousand angstrom titanium layer formed on the silicon wafer, with the composite layers of ferroelectric material deposited thereover. On wafer 7037B, the titanium layer was removed, and thus the ferroelectric composite layer was deposited directly on the spin-on oxide. With wafer 7037C, only 500 angstroms of titanium were deposited on the spin-on oxide. Wafer 7037D was a control wafer, in which a thousand angstroms of titanium was formed on the spin-on oxide, but only a single type, rather than a composite layer, of ferroelectric material was utilized.
- 19. Wafer 7037E was a wafer obtained from Orbit Semiconductor and cut into quarters for processing according to different tests. One quarter of the wafer had silicon nitride formed on a silicon dioxide, and a "209" oxide formed over the nitride. Wafer 7037F was processed

similarly, except that it underwent a hydrogen fluoride dip. Wafer 7037G was similarly processed, but with two coats of the 209 oxide over the silicon nitride. Wafer 7038A was also similarly processed, but with one type of ferroelectric material rather than a composite material layer. These wafers obtained from Orbit were believed to have been etched to provide a specified topography which was used as a parameter during the wafer processing tests. Also, some of the wafers underwent a sintering operation, while others did not.

- 20. Other examples of wafer tests include film ID 7043B which was a TD01 CMOS test wafer processed with a single composition of ferroelectric material on February 12, 1987. This wafer had a thin titanium layer over the wafer silicon dioxide, with no capacitor bottom electrode.
- 21. On February 13, 1987, wafer 7044A, which was a CMOS transistor type of wafer, was processed with a standard bottom electrode material, covered with an 8/40/60 composition of ferroelectric material. The wafer was then cut into 1" squares for lift-off dot mask (LODM) tests. Also, wafer 7044B included a standard bottom electrode material, covered with 250 angstroms of titanium and 1500 angstroms of platinum. Many other wafers were prepared on February 13, 1987, as noted in the log.
- 22. On February 17, 1987, wafer 7048A was prepared with a composition of ferroelectric material, but rather than sintering in an oxygen ambient, such wafer was both annealed in an argon gas, as well as sintered in an argon gas.

- 23. On February 25, 1987, wafer 7056A-1 was prepared with a ferroelectric material and annealed immediately after coating thereof.
- 24. On February 25, 1987, wafer 7056A-1 was dipped in a nitric acid after annealing to roughen the surface to determine if a better adhesion of the ferroelectric material was achieved.
- 25. Wafer 7056A-2 was prepared with a ferroelectric material on February 25, 1987, and annealed for 72 hours.
- 26. Wafer 7056A-3 was prepared with a ferroelectric material and a top electrode, and then subjected to an R10 resist stripper and then annealed. This test is believed to be carried out to determine the adhesion capability of the top electrode material following the application of the resist stripper thereto. The resist stripper is utilized in patterning the ferroelectric material. 7056A-4 was similarly processed, but the wafer was soaked in the R10 resist stripping solution for twice the amount of time.
- 27. Wafer 7056A-6 was prepared with eight coats of a ferroelectric material and then subjected to an acetone and isopropanol solution, and then immediately annealed.
- 28. On February 25, 1987, wafer 7056A-7 was also prepared with eight coats of a ferroelectric material, and subjected to another type of stripper, denoted "130".
- 29. On February 25, 1987, wafer 7056A-8 was tested as to a top electrode, by use of a spin-on platinum material.

- 30. On February 28, 1987, wafer 7059A was prepared with eight coats of an 8/40/60 ferroelectric material and tested with isopropanol supplied by Alfa. I recall that one lot of isopropanol from that supplier caused the synthesis of a sol-gel to be ruined, and thus the present test was to test a new lot of isopropanol on a new sol-gel ferroelectric material.
- 31. Wafer 7069A was coated with a ferroelectric material on March 10, 1987, to conduct a test of a new top electrode technique, termed "Fatl". With the Fatl wafer structures, both the top electrode and the bottom electrode of the ferroelectric capacitor were accessible for tests, whereas in the LODM structure, two ferroelectric capacitors were formed in series, with only the outer terminals being accessible, and the inner common terminal was not accessible for testing.

On March 16, 1987, wafer 7075C was prepared with a ferroelectric composition, but not sintered. Other wafers were prepared on such date but sintered at 650°C. The sintered and unsintered wafers were utilized by Krysalis to align and adjust a new semiconductor processing stepper machine purchased from ASM. Such a stepper utilized a laser for aligning the masks to the wafer. The sintered and unsintered wafers exhibited different crystal structures and thus different indices of refraction for aligning the stepper.

32. As noted on page 14 of the log, during March 16, 17 and 18, 1987, numerous different types of ferroelectric compositions, including 3/40/60; 0/50/50; 15/0/100; and 3/60/40 were utilized as different parameters to determine performance characteristics.

- 33. On March 23, 1987, wafer 7082A was processed with different layers of ferroelectric material to determine which composition exhibited the least cracking during high temperature processing. Particularly, a 15/0/100 composition of ferroelectric material was deposited and then thereover an 8/40/60 composition of ferroelectric material. Such tests were conducted on Orbit test wafers, as well as CMOS wafers, and on both the LODM and Fatl top electrode structures.
- 34. On March 27, 1987, wafer 7086A was prepared with a blend of ferroelectric materials. In these tests, the ferroelectric sol-gels were actually mixed together in liquid form to arrive at a composite resultant ferroelectric material.
- 35. On March 30, 1987, and April 3, 1987, wafers 7089B and 7093A,B were prepared respectively with ferroelectric compositions to conduct a top electrode barrier study. According to this study, efforts were expended to eliminate reactions of aluminum contacts with platinum. It was found that by depositing a titanium layer over the platinum, and then aluminum over the titanium, the adverse material reaction between aluminum and platinum was reduced.
- 36. On April 4, 1987, a number of wafers were prepared, starting with wafer 7094A to conduct a scratch protection study. In this study, experiments were conducted to select a top passivation layer for covering the ferroelectric capacitors. It is believed that different spin-on glasses, silox and other depositions of materials were used as the passivation layer. As can be seen on the bottom of page 15 of the log, different ramp-in/out parameters were utilized to determine optimum results. In

other words, the speed at which the wafers were fed on a conveyor into the diffusion furnace was varied to vary the temperature gradient to which the wafers were exposed. Many materials adversely react with the ferroelectric material, and thus the selection of a passivation layer was significant in fabricating ferroelectric memories. Not only do various materials chemically react with ferroelectric material, but such materials can also place a mechanical stress on the ferroelectric material. Because the ferroelectric material exhibits piezoelectric properties, external stresses can change the characteristics of the ferroelectric material.

- 37. On April 6, 1987, wafers 7096C and D were prepared with an 8/40/60 composition of ferroelectric material, but with different amounts of excess lead. These wafers were prepared to conduct an excess lead study. As noted in the FES coating log, wafer 7096C was prepared with a ferroelectric material having no excess lead, while wafer 7096D was prepared having 30 parts of excess lead.
- 38. On April 7 and 8, 1987, a number of TD01 CMOS wafers were prepared with different compositions of ferroelectric material, as well as other different parameters, to conduct pre-512 process tune-up. The TD01 CMOS wafers were processed through the Krysalis processing equipment to determine the correct operation thereof before processing the more expensive ECD512 CMOS wafers. The TD01 CMOS wafers are identified at pages 16 and 17 of the log, starting with wafer 7097B.

- 39. On April 8, 1987, a number of ECD512 test wafers were prepared, starting with 7098E. These test wafers had no CMOS memory circuits, but underwent a pre-etch to provide a topography similar to a ECD512 wafer with CMOS memory circuits. The ECD512 test wafers bearing film IDs 7098E-7100B were processed with different parameters, such as some having eight coats of ferroelectric material, while wafer 7098G had 32 coats. Also, the ferroelectric material on some of the wafers was deposited over a single spin-on layer of titanium, while other wafers had the ferroelectric material deposited over two such layers of the titanium material. In addition, some wafers underwent an oxidation cycle at 650°C, while others were subjected to an oxidizing environment of 750°C.
- 40. ECD512A wafers 7105A,D were prepared on April 15, 1987, with a ferroelectric material. These wafers were fabricated at Orbit Semiconductor with CMOS memory transistors and circuits.
- 41. On April 16, 1987, wafers 7106C, D and E were prepared with different ferroelectric compositions for test evaluation purposes. Particularly, wafer 7106C had a blend of G7072 and G7090A ferroelectric material, yielding a 5.5/40/60,+5 resulting composition. Wafer 7106D was prepared with a 50:50 blend of G7072 and G7055 ferroelectric material, resulting in a composition of 5.5/40/60,+10. Wafer 7106E was prepared with a 1/2:1/6:1/3 blend of G7072 and 7090A and 7091 ferroelectric sol-gels which resulted in a 5.5/40/60,+15 resultant blend. The excess lead compositions for each of the blends differed, thus providing materials for evaluating with respect to ferroelectric properties.

- 42. On April 24, 1987, yet other wafers were prepared, starting with wafer 7114A to conduct a bottom electrode study. In this study, different thicknesses of titanium dioxide were deposited under the bottom electrode which comprised 500 angstroms of titanium and 1000 angstroms of platinum.
- 43. On April 27, 1987, TD01 CMOS wafer 7117A was processed with a layer of ferroelectric material for conducting yet another bottom electrode study. On the same date, an ECD512 wafer with CMOS memory circuits (7117B) was processed with a layer of ferroelectric material, to also conduct a bottom electrode test.
- 44. On April 30, 1987, wafers 7120B-D were prepared with the same composition of ferroelectric material to conduct an interlevel dielectric (ILD) study. The interlayer dielectric comprised a spin-on oxide deposited over the top electrode of the ferroelectric capacitor.
- 45. On May 1, 1987, wafers 7121A-C were prepared with a composition of ferroelectric materials to conduct a buffer layer study. Two different ferroelectric sol-gels were deposited in different layers with an intermediate buffer layer to determine the extent of blistering after the sintering operation.

46. On May 5, 1987, wafers 7125A and B were processed with ferroelectric material, but were not annealed, to conduct tests for aligning the wafer processing stepper equipment.

- 47. On May 5, 1987, ECD512A wafer 7125F was prepared with eight coats of a ferroelectric material to conduct tests on the non-volatile ferroelectric memory cells.
- 48. On May 11, 1987, a Fatl wafer (7131A) was prepared with eight coats of a ferroelectric composition 3/60/40 to conduct fatigue tests thereon.
- 49. On May 12, 1987, wafer 7132A was prepared with a ferroelectric material to conduct ion gun etch studies. This evaluation was to determine the effect of ion etching on ferroelectric material, rather than the standard use of wet etching solutions.
- 50. On May 15, 1987, ECD512A wafers 7135B,C and 7139A were prepared with ferroelectric compositions, and thereafter tested to determine the electrical characteristics of the non-volatile memory cells.
- 51. On May 22, 1987, wafers 7142A,B were prepared with a new sol-gel ferroelectric composition, defined as 0/50/50,+10.
- 52. On May 28, 1987, ECD512A wafers having CMOS memory circuits, identified as film IDs 7148A,B, were prepared with different ferroelectric materials to be evaluated accordingly.

53. On June 1, 1987, wafer 7152A was prepared with compositions of ferroelectric materials having buffer layers therebetween. On the same day, wafers 7152C and D were processed with ferroelectric materials to conduct a film thinness study.

- 54. On June 4, 1987, wafers 7155A-C were prepared with new compositions of ferroelectric material, namely 0/50/50; 1/45/55 and 0/40/60 to conduct electrical tests of the ferroelectric material.
- 55. As noted on pages 20-28 of the FES coating log, many other wafers were prepared with ferroelectric materials for conducting tests subsequent to June 5, 1987.
- 56. Exhibit B is a copy of my memorandum dated June 16, 1987, concerning failure rate studies of numerous chips, or die, cut from the CMOS ECD512A wafer identified as Film ID 7148A. As noted in the log of Exhibit A, such wafer was processed with a ferroelectric material on May 28, 1987, and tested by Mr. David Eaton, also a Krysalis employee, who provided the bit failures of six of the die cut from the wafer.
- 57. On information and belief, electrical tests on the wafers noted above were actually carried out by Krysalis personnel.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Date: Jul 28,1991 Leo N. Chapin

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t°C/%RH @ Spln										·													
COATS & SPIN	cts @ rpm	10cts @ 2000rpm	10cts @ 2000rpm	10cts @ 2000rpm	10cts @ 2000rpm	10cts @ 2000rpm	10cts @ 2000rpm	10cts @ 2000rpm	10cts @ 2000rpm	10cts @ 2000rpm	10cts @ 2000rpm	10cts @ 2000rpm	10cts @ 2000rpm	10cts @ 2000rpm	10cts @ 2000rpm	10cts @ 2000rpm	10cts @ 2000rpm	10cts @ 2000rpm	10cts @ 2000rpm	10cts @ 2000rpm	10cts @ 2000rpm	10cts @ 2000rpm	10cts @ 2000rpm
SOL-GEL ID, (Composition), & AGE in days	G, (),	G6192, (8/40/60,+10), 22	G6208, (8/40/60,+10), 6	G6210, (3/40/60,+10), 4	G6210, (3/40/60,+10), 4	G6210, (3/40/60,+10), 4	G6213, (3/60/40,+10), 1	G6208, (8/40/60,+10), 10	G6210, (3/40/60,+10), 8	G6213, (3/60/40,+10), 5	G6208, (8/40/60,+10), 16	G6210, (3/40/60,+10), 14	G6213, (3/60/40,+10), 11	G6208, (8/40/60,+10), 16	G6213, (3/60/40,+10), 11	G6208, (8/40/60,+10), 16	G6210, (3/40/60,+10), 14	G6213; (3/60/40,+10), 11	G6208, (8/40/60,+10), 16	G6210, (3/40/60,+10), 14	G6213, (3/60/40,+10), 11	G6213, (3/60/40,+10), 14	G6208, (8/40/60,+10), 25
BEL		810	B10	Pt#10	Pd#1	B10	B10	B10	B10	B 10	118	B 11	B11	B 11	B 11	B 11	B11	118	B11	B11	B11	B10	Pt#12
SUBSTRATE DESCRIPTION		2/86 Si 1/4 Wafer 10min-625°C anneal	2/86 Si 1/4 Wafer 10min-625°C anneal.	2/86 Pt#10 10min-625°C anneal.	2/86 Pd#1 10min-625°C anneal.	2/86 Si Wafer 10min-625°C anneal.	2/86 Si 1/4 Wafer 10min-625°C anneal.	6/86 Si 1/4 Wafer 120min-625°C anneal.	6/86 Si 1/4 Wafer 120min-625°C anneal	5/86 Si 1/4 Wafer 120min-625°C anneal	2/86 Si 1/4 Wafer 10min-625°C anneal.	2/86 Si 1/4 Wafer 10min-625°C anneal.	2/86 Si 1/4 Wafer 10min-625°C anneal.	2/86 Si 1/4 Wafer 30min-625°C anneal.	2/86 Si 1/4 Wafer 30min-625°C anneal.	2/86 Si 1/4 Wafer 30min-600°C anneal.	2/86 Si 1/4 Wafer 30min-600°C anneal.	2/86 Si 1/4 Wafer 30min-600°C anneal	2/86 Si 1/4 Wafer 60min-600°C anneal	2/86 Si 1/4 Wafer 60min-600°C anneal	2/86 Si 1/4 Wafer 60min-600°C anneal.	5/86 Si Wafer 30min-625°C anneal.	Pt#12
DATE COATED	:	08/02/86 10min	08/02/86 10min	08/02/86 10min	08/02/86 10min	08/02/86 10min	08/02/86 10min	08/06/86 120mi	08/06/86 120mi	08/06/86 120mi	08/12/86 10min	08/12/86 10min	08/12/86 10min	08/12/86 30min	08/12/86 30min	08/12/86 30min	08/12/86 30min	08/12/86 30min	08/12/86 60min	08/12/86 60min	08/12/86 60min	08/15/86 30min	08/21/86
FILM	F6060	F6107	F6109	F6110	F6111	F6113	F6115	F6117	F6119	F6120	F6121	F6122	F6123	F6124	F6127	F6128	F6129	F6130	F6131	F6132	F6134	F6135	F6136

FILM	DATE	SUBSTRATE DESCRIPTION	TE BEL ON TYPE	SOL-GEL ID, (Composition), & AGE in	COATS & SPIN In days SPEED	t°C/%RH @ Spin	BAKE PROFILE	SINTER PROFILE	TEL TYPE
F6137	08/27/86 30min-	7/86 1/4wafer 30min-600°C anneal. (B10or11 G6208 is old CODE G620.	G6208, (8/40/60,+10), DDE G620.), 12cts @ 2000rpm		¥.	550°sinter	٠
F6138	08/28/86 30min-	8/86 1/4wafer 30min-600°C anneal. (B10or11 G6208 is old CODE G620.	G6208, (8/40/60,+10), DDE G620.), 8cts @ 2000rpm		¥	550°sinter	~
F6139	08/28/86 30min-	8/86 1/4wafer 30min-600°C anneal. (B10or11 G6208 is old CODE G620.	G6208, (8/40/60,+10), DDE G620.), 6cts @ 2000rpm		¥	550°sinter	~
F6140	08/27/86 60min-		Pt#1 G6208 is old CODE G620	G6208, (8/40/60,+10), DDE G620.), 10ⴛs @ 2000rpm		¥	550°sinter	~
F6141	08/27/86 30min-		Pt#3 G6208 is old CODE G620	G6208, (8/40/60,+10), DDE G620.), 10cts @ 2000rpm		¥	550°sinter	~
6220B	08/08/80	Si Wafer	B11	G6208, (8/40/60,+10),), 10cts @ 2000rpm		¥	550°sinter	~
6247A	09/04/86 30min-	4/86 Si Wafer B19 G6 30min-625°C anneal. G6208 is old CODE G620.	B19 G6208 is old CC	G6208, (8/40/60,+10), 39 DDE G620.	39 10cts @ 2000rpm		¥	550°sinter	~
6247B	09/04/86 30min-	4/86 Si Wafer 30min-625°C anneal.	B17 G6208 is old CODE G620.	G6208, (8/40/60,+10), 39 DDE G620.	39 10cts @ 2000rpm		¥	550°sinter	~
6247C	09/04/86 30min-	4/86 Si Wafer 30min-625°C anneal.	B17 G6208 is old CODE G620.	G6208, (8/40/60,+10), 39 ODE G620.	39 10cts @ 2000rpm		¥.	550°sinter	~
6247D	09/04/86 30min-	4/86 Si Wafer 30min-625°C anneal.	B18 G6208 is old CODE G620.	G6208, (8/40/60,+10), 39 ODE G620.	39 10cts @ 2000rpm		¥	550°sinter	c-
6247E	09/04/86 30min-	4/86 Si Wafer 30min-625°C anneal.	B18-patt G6208 is old CODE G620.	G6208, (8/40/60,+10), 39 ODE G620.	39 10cts @ 2000rpm		¥	550°sinter	~
6247F	09/04/86 30min-	4/86 Si Wafer 30min-625°C anneal.	B17-patt G6208 is old CODE G620.	G6208, (8/40/60,+10), 39 ODE G620.	39 10cts @ 2000rpm		¥	550°sinter	Č
6247G	09/04/86 30min-	4/86 Si Wafer 30min-625°C anneal.	B17-patt G6208 is old CODE G620.	G6208, (8/40/60,+10), 39 ODE G620.	39 10cts @ 2000rpm		¥	550°sinter	~
6247H	09/04/86 30min-	4/86 Si Wafer 30min-625°C anneal.	B17-patt G6208 is old CODE G620.	3208,	39 10cts @ 2000rpm		ž	550°sinter	~
62471	09/04/86 30min-	4/86 Si Wafer 30min-625°C anneal.	B17-patt G6208 is old CODE G620.	G6208, (8/40/60,+10), 39 ODE G620.	39 10cts @ 2000rpm		ş	550°sinter	<i>د</i>
6247J	09/04/86 30min-	4/86 Si Wafer 30min-625°C anneal.	B17-patt G6208 is old CODE G620.	G6208, (8/40/60,+10), 39 ODE G620.	39 10cts @ 2000rpm		≨	550°sinter	~
6247K	09/04/86 30min-	4/86 Si Wafer 30min-625°C anneal.	B18-patt G6208 is old CODE G620.	G6208, (8/40/60,+10), 39 ODE G620.	39 10cts @ 2000rpm		¥	550°sinter	~
6247L	09/04/86 30min-	4/86 Si Wafer 30min-625°C anneal.	B18-patt G6208 is old CODE G620.	6208,	.39 10cts @ 2000rpm		¥	550°sinter	~
6248A	09/05/86 30min-	5/86 Si Wafer 30min-600°C anneal.	B19 G G6208 is old CODE G620	G6208, (8/40/60,+10), 40 ODE G620.	. 40 10cts @ 2000rpm		¥	550°sinter	<i>~</i>
6248B	09/05/86 30min-	5/86 Si Wafer 30min-600°C anneal.	B17 G6210 is old CODE G621.	G6210, (3/40/60,+10), 38 ODE G621.	.38 10cts @ 2000rpm		¥	550°sinter	~
6248D	09/05/86 30min-	Si Wafer -600°C anneal,1	B19-patt 10"/min ramp. G	5/86 Si Wafer B19-patt G6208, (8/40/60,+10), 40 30min-600°C anneal,10"/min ramp. G6208 is old CODE G620.	, 40 10cts @ 2000rpm		¥	550°sinter	~
6252A	09/09/86 30min-	9/86 Si Wafer 30min-600°C anneal.	B20 G6 G6208 is old CODE G620.	G6208, (8/40/60,+10), 44 ODE G620.	, 44 10cts @ 2000rpm		¥	550°sinter	٠
6252B	09/09/86 30min	9/86 Si Wafer B16-patt G/ 30min-600°C anneal. G6208 is old CODE G620.	B16-patt G6208 is old C	t G6208, (8/40/60,+10), 44 ODE G620.	, 44 10cts @ 2000rpm		ş	550°sinter	~

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TEL TYPE	ć	~	~	~	٠	~	~	٠	٠	~	~	~	~	~	~	~	~	٠	٠	٠	~	~	~
SINTER	550°sinter	550°sinter	550°sinter	550°sinter	550°sinter	550°sinter	550°sinter	550°sinter	550°sinter	550°sinter	550°sinter	550°sinter	550°sinter	550°sinter	550°sinter	550°sinter	550°sinter	550°sinter	550°sinter	550°sinter	550°sinter	550°sinter	550°sinter
BAKE PROFILE	NA	¥	¥	ž	¥	ž	¥	¥	¥	¥	¥	≨	¥	¥	¥	¥	¥	¥	¥	¥	¥	¥	¥
t°C/%RH @ Spin																							
COATS & SPIN SPEED	10cts @ 2000rpm	10cts @ 2000rpm	10ⴛა @ 2000грო	10cts @ 2000rpm	10cts @ 2000rpm	10cts @ 2000rpm	10cts @ 2000rpm	10cts @ 2000rpm	10cts @ 2000rpm 0.	10cts @ 2000rpm 0.	10cts @ 2000rpm	10cts @ 2000rpm	10cts @ 2000rpm	10cts @ 2000rpm 20.	10cts @ 2000rpm 0.	10cts @ 2000rpm 0.	10cts @ 2000rpm 0.	10cts @ 2000rpm	10cts @ 2000rpm 20.	8cts @ 2000rpm	8cts @ 2000rpm	8cts @ 2000rpm	8cts @ 2000rpm
SOL-GEL ID, (Composition), & AGE in days	G6208, (8/40/60,+10), 44)E G620.	G6208, (8/40/60,+10), 44)E G620.	G6251, (8/40/60,+10), 1)E G623.	G6251, (8/40/60,+10), 1)E G623.	G6210, (3/40/60,+10), 42)E G621.	G6210, (3/40/60,+10), 42)E G621.	G6210, (3/40/60,+10), 42)E G621.	G6251, (8/40/60,+10), 1 251 is old CODE G623.	G6208, (8/40/60,+10), 46 rol for 6254F. G6208 is old CODE G620.		G6208, (8/40/60,+10), 46 38 is old CODE G620.	G6208, (8/40/60,+10), 46 38 is old CODE G620.	G6210, (3/40/60,+10), 44 10 is old CODE G621.	G6208, (8/40/60,+10), 46 A-H2O2 clean. G6208 is old CODE G620.	G6208, (8/40/60,+10), 46 -H2O2 clean. G6208 is old CODE G620.		G6208, (8/40/60,+10), 46 -H2O2 clean. G6208 is old CODE G620.	G6208, (8/40/60,+10), 46 08 is old CODE G620.	G6208, (8/40/60,+10), 46 A-H2O2 clean. G6208 is old CODE G620.	G6208, (),	G6208, (),	G6251, (),	G6251, (),
TE SUBSTRATE BEL	Si Wafer in-600°C anneal.	9/86 Si Wafer B20-patt G6208, (30min-600°C anneal. G6208 is old CODE G620.	Si Wafer in-600°C anneal.	Si Wafer in-600°C anneal.	Si Wafer in-600°C anneal.	Si Wafer in-600°C anneal.	9/86 Si Wafer B21-patt G 30min-600°C anneal. G6210 is old CODE G621	9/86 Si Wafer B16 G6251, (8/40/6/ 30min-600°C anneal,10"/min ramp. G6251 is old CODE G623.	1/86 Si Wafer B22-patt G6208 30min-600°C anneal,10*/min ramp;control for 6254F.	1/86 Si Wafer B22-patt G6208 30min-600°C anneal, 10"/min ramp;control for 6254F.	1/86 Si Wafer B22-patt G6208, (30min-600°C anneal,5"/min ramp. G6208 is old CODE	1/86 Si Wafer B22-patt G6208, 030min-600°C anneal,5"/min ramp. G6208 is old CODE	1/86 Si Wafer B22-patt G6210, (30min-600°C anneal,5"/min ramp. G6210 is old CODE	1/86 Si Wafer B22-patt G6208, 30min-600°C anneal, 10"/min ramp; EDTA-H2O2 clean.	1/86 Si Wafer B22-patt G6208. 30min-600°C anneal,5"/min ramp;EDTA-H2O2 clean.	1/86 Si Wafer B22-patt G6208 30min-600°C anneal,5"/min ramp;EDTA-H2O2 clean.	1/86 Si Wafer B22-patt G6208 30min-600°C anneal,5'/min ramp;EDTA-H2O2 clean.	1/86 Si Wafer B21-patt G6208, (30min-600°C anneal,5"/min ramp. G6208 is old CODE	1/86 Si Wafer B19-patt G6208, 30min-600°C anneal, 10"/min ramp;EDTA-H2O2 clean.	2/86 Si Wafer B23-patt 30min-600ÅC anneal,10"/min ramp	2/86 Si Wafer B23-patt 30min-600ÅC anneal,10"/min ramp	2/86 Si Wafer B23-patt 30min-600AC anneal,10"/min ramp	2/86 Si Wafer B23-patt 30min-600AC anneal,10"/min ramp
FILM DATE ID COATED	6252C 09/09/86 30m	6252D 09/09/86 30m	6252E 09/09/86	6252F 09/09/86 30m	6252G 09/09/86	6252H 09/09/86	6252 09/09/86 30m	6252J 09/09/86 30m	6254A 09/11/86	6254B 09/11/86	6254C 09/11/86 30mi	6254D 09/11/86	6254E 09/11/86	6254F 09/11/86	6254G 09/11/86	6254H 09/11/86	62541 09/11/86	6254J 09/11/86	6254K 09/11/86	6255A 09/12/86	6255B 09/12/86	6255C 09/12/86	6255D 09/12/86

FILM	DATE	SUBSTRATE DESCRIPTION	BEL TYPE	SOL-GEL ID, (Composition), & AGE in days	COATS & SPIN	t°C/%RH @ Spin	BAKE PROFILE	SINTER PROFILE	TEL TYPE
6255E	09/12/86 30min-	2/86 Si Wafer B23-pat 30min-600ÅC anneal,10"/min ramp.	B23-patt min ramp	G6251, (),	8cts @ 2000rpm		¥	550°sinter	ć
6258A	09/15/86 30min-	5/86 Si Wafer B25-pat 30min-600ÅC anneal,10"/min ramp.	B25-patt min ramp.	G6208, (8/40/60,+10), 58	8cts @ 2000rpm		ž	550°sinter	٠
6258B	09/15/86 30min-	5/86 Si Wafer B25-pat 30min-600ÅC anneal,10"/min ramp.	B25-patt min ramp.	G6208, (8/40/60,+10), 58	8cts @ 2000rpm		ž	550°sinter	٠
6258C	09/15/86 30min	5/86 Si Wafer B23-pat 30min-600ÅC anneal,10*/min ramp.	B23-patt min ramp.	G6208, (8/40/60,+10), 58	8cts @ 2000rpm		¥	550°sinter	~
6258D	09/15/86 30min	5/86 Si Wafer B25-pat 30min-600ÅC anneal,10"/min ramp.	B25-patt min ramp	G6251, (8/40/60,+10), 7	8cts @ 2000rpm		¥	550°sinter	٠
6258F	09/15/86 30min	5/86 Si Wafer B23-pat 30min-600ÅC anneal,10"/min ramp.	B23-patt min ramp	G6251, (8/40/60,+10), 7	8cts @ 2000rpm		¥	550°sinter	٠
6258G	09/15/86 30min	5/86 Si Wafer B25-pa/ 30min-600ÅC anneal,10"/min ramp.	B25-patt min ramp.	G6251, (8/40/60,+10), 7	8cts @ 2000rpm		ž	550°sinter	~
6260A	09/17/86 30min	7/86 Si Wafer B25-patt 30min-600ÅC anneal,10"/min ramp;control.	B25-patt min ramp;∞nt	G6251, (8/40/60,+10), 9 Irol	8cts @ 2000rpm		ž	550°sinter	٠
6260B	09/17/86 30min	7/86 Si Wafer B26-patt 30min-600ÅC anneal,10"/min ramp;control.	B26-patt min ramp;cont	G6251, (8/40/60,+10), 9 Irol	8cts @ 2000rpm		ž	550°sinter	٠
6260C	09/17/86 30min	7/86 Si Wafer B26-patt G6251, 30min-600ÅC anneal,10"/min ramp;EDTA-H2O2 clean.	B26-patt min ramp;EDT,	G6251, (8/40/60,+10), 9 A-H2O2 clean.	8cts @ 2000rpm		¥	550°sinter	~
6260D	09/17/86 30min	7/86 Si Wafer B26-patt G6251, 30min-600ÅC anneal,10"/min ramp;EDTA-H2O2 clean.	B26-patt min ramp;EDT,	G6251, (8/40/60,+10), 9 A-H2O2 clean.	8cts @ 2000rpm		¥	550°sinter	٠
6260E	09/17/86 30min	7/86 Si Wafer B26-patt G6251, 30min-600ÅC anneal, 10"/min ramp;EDTA-H2O2 clean.	B26-patt min ramp;EDT,	G6251, (8/40/60,+10), 9 A-H2O2 clean.	8cts @ 2000rpm		¥	550°sinter	۷
6260F	09/17/86 30min	7/86 Si Wafer B26-patt G6251, 30min-600ÅC anneal,10"/min ramp;EDTA-H2O2 clean.	B26-patt min ramp;EDT	G6251, (8/40/60,+10), 9 A-H2O2 clean	8cts @ 2000rpm		¥	550°sinter	٧
6260G	09/17/86 30min	7/86 Si Wafer B25-patt G6251, 30min-600ÅC anneal,10*/min ramp;EDTA-H2O2 clean.	B25-patt min ramp;EDT,	G6251, (8/40/60,+10), 9 A-H2O2 clean	8cts @ 2000rpm		¥	550°sinter	٠
6260H	09/17/86 Blister	7/86 TINitride None Blistered and cracked after 1st coat sinter.	None er 1st coat sint	G6251, (8/40/60,+10), 9 ter	1cts @ 2000rpm		¥	550°sinter	~
6261A	09/18/86 30min	8/86 Si Wafer 30min-600ÅC anneal.	B25,5-55p	G6210, (3/40/60,+10), 51	8cts @ 2000rpm		¥	550°sinter	~
6261B	09/18/86 30min	8/86 Si Wafer 30min-600ÅC anneal	B25,6-55p	G6251, (8/40/60,+10), 10	8cts @ 2000rpm		¥	550°sinter	~
6261C	09/18/86 30min	8/86 Si Wafer 30min-600ÅC anneal.	B26,1-60p	G6251, (8/40/60,+10), 10	8cts @ 2000rpm		¥	550°sinter	٠
6261D	09/18/86 30min	8/86 Si Wafer 30min-600ÅC anneal.	B26,2-70p	G6251, (8/40/60,+10), 10	8cts @ 2000rpm		¥	550°sinter	٠
6261E	09/18/86 30min	8/86 Si Wafer 30min-600ÅC anneal.	B26,4-60p	G6251, (8/40/60,+10), 10	8cts @ 2000rpm		ž	550°sinter	٠
6261F	09/18/86 30min	8/86 Si Wafer 30min-600ÅC anneal	B27,2patt	G6251, (8/40/60,+10), 10	8cts @ 2000rpm		ž	550°sinter	۰
6261G	09/18/86 30min	8/86 Si Wafer 30min-600AC anneal	B27,3patt	G6251, (8/40/60,+10), 10	8cts @ 2000rpm		¥	550°sinter	~
6261H	09/18/86 30min	8/86 Si Wafer 30min-600AC anneal.	B27,4patt	G6251, (8/40/60,+10), 10	8cts @ 2000rpm		¥	550°sinter	~

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0,+10), 25	10cts @ 2000rpm	§	550°sinter	٤
	22Feb91 reprint of FES coating log (last modified Wed, Nov 4, 1987 4:11pm. Page 5	(last modified V	Ved, Nov 4, 1987 4:11	pm. Page 5

TEL TYPE	~	~	~	٠	~	~	~	,	٠,	~	٠	٠	~	~	~	~	~	~	٠	~	~	٠	~
SINTER PROFILE	550°sinter	550°sinter	550°sinter	550°sinter	550°sinter	550°sinter	550°sinter	550°sinter	550°sinter	550°sinter	550°sinter	550°sinter	550°sinter	550°sinter	550°sinter	550°sinter	550°sinter	550°sinter	550°sinter	550°sinter	550°sinter	550°sinter	550°sinter
SIS	250	550	550	550	520	520,	520	550	220,	520	550	550	520	550	550,	550	550	220,	550,	550	550	550	220
BAKE PROFILE	¥	¥	≨	¥	₹	¥	¥	¥	¥	¥	¥	₹	≨	₹	¥	≨	₹	≨	₹	¥	¥	¥	≨
PRO	2	_	2	2	2	2	_	_	_	_	2	_	2	2	-	2	_	_	_	_	_	_	_
t°C/%RH @ Spln																							
& SPIN	00rpm	00rpm	00rpm	000rpm	000rpm	000rpm	000rpm	300rpm	000rpm	000rpm	000rpm	000rpm	000rpm	00rpm	.00rpm	mq100	00rpm	000rpm	000rpm	300rpm	300rpm	000rpm	D00rpm
COATS &	8cts @ 2000rpm	8cts @ 2000rpm	8cts @ 2000rpm	10cts @ 2000rpm	10cts @ 2000rpm	10ds @ 2000rpm	10¢s @ 2000rpm	10cts @ 2000rpm	10ძა @ 2000rpm	10cts @ 2000rpm	10cts @ 2000rpm	10cts @ 2000rpm	10cts @ 2000rpm	8cts @ 2000rpm	8cts @ 2000rpm	8cts @ 2000rpm	8cts @ 2000rpm	10cts @ 2000rpm	10ds @ 2000rpm	10cts @ 2000rpm	10cts @ 2000rpm	10cts @ 2000rpm	10cts @ 2000rpm
C In days																					-		
ID, AGE In	(8/40/60,+10), 10	(8/40/60,+10), 10	(10/40/60,+10), 6	(8/40/60,+10), 16	(8/40/60,+10), 16	(8/40/60,+10), 16	(8/40/60,+10), 16	(8/40/60,+10), 16	(8/40/60,+10), 16	(10/40/60,+10), 12	(6/40/60,+10), 14	(6/40/60,+10), 14	(6/40/60,+10), 14	G6251, (8/40/60,+10), 21	G6251, (8/40/60,+10), 21	G6251, (8/40/60,+10), 21	(8/40/60,+10), 21	G6251, (8/40/60,+10), 22	(8/40/60,+10), 22	G6251, (8/40/60,+10), 22	(8/40/60,+10), 22	(8/40/60,+10), 22	(8/40/60.+10). 25
SOL-GEL ID,	(8/40/60	, (8/40/60			, (8/40/60	, (8/40/60	, (8/40/60	, (8/40/60	, (8/40/60	(10/40/6		, (6/40/60		, (8/40/60	, (8/40/60	, (8/40/60	, (8/40/60	, (8/40/60	, (8/40/60	, (8/40/60		, (8/40/60	
SOL-GEL	G6251,	G6251,	G6255,	G6251,	G6251,	G6251,	G6251,	G6251,	G6251,	G6255,	G6253	G6253,	G6253	G6251	G6251	G6251	G6251,	G6251	G6251,	G6251	G6251,	G6251,	G6251,
BEL TYPE (=	B27,6patt	B25,3-65p	1/4B28	1/4B28pat	1/4B28pat	B28patt	B28patt	B28patt	B28patt	B28patt	B28patt	B28patt	B23	B23	B27	B27	B17	B19	B21	B27	B27rnd	B29
		B27,	B25,	4	1/48	1/48	B28	B 28	B26	828	B28	B28	B28	æ	Φ.	₩.	&	6	a	a	<u>ш</u>	82	a
SUBSTRATE DESCRIPTION	Si Wafer Sanneal.	Si Wafer	Si Wafer Sanneal.	OrbNitride C anneal.	OrbNitride C anneal	OrbNitride C anneal	2°CVD Nit C anneal.	2"CVD Nit C anneal.	2°CVD Nit C anneal.	VD Nit	VD Nit	2"Oxide sanneal.	2"Oxide sanneal	Si Wafer Sanneal.	Si Wafer Sanneal.	Si Wafer Sanneal.	Si Wafer Sanneal.	Si Wafer	Si Wafer	Si Wafer	Si Wafer	Si Wafer	Si Wafer.sor
SUB: DESC	8/86 Si Wafer 30min-600AC anneal.	Si neal	8/86 Si Wafer 30min-600AC anneal.	4/86 OrbNitride 30min-600AC anneal.	4/86 OrbNitride 30min-600AC anneal.	4/86 OrbNitride 30min-600ÅC anneal.	4/86 2°CVD Ni 30min-600ÅC anneal.	4/86 2°CVD Nii 30min-600AC anneal.	4/86 2°CVD Ni 30min-600ÅC anneal.	4/86 2°CVD Nit 30min-600AC anneal.	4/86 2°CVD Nit 30min-600AC anneal.	4/86 2"Oxide 30min-600ÅC anneal.	4/86 2"Oxide 30min-600ÅC anneal.	9/86 Si Wafer 30min-600ÅC anneal.	9/86 Si Wafer 30min-600ÅC anneal.	9/86 Si Wafer 30min-600AC anneal.	9/86 Si Wafer 30min-600AC anneal.	ιΩ	ଊ	জ	ଊ	ัง	× Si
DATE COATED	09/18/86 30min	09/18/86 No anneal.	09/18/86 30min	09/24/86 30min	09/24/86 30min	09/24/86 30min	09/24/86 30min	09/24/86 30min	09/24/86 30min	09/24/86 30min	09/24/86 30min	09/24/86 30min	09/24/86 30min	09/29/86 30min	09/29/86 30min	09/29/86 30min	09/29/86 30min	98/06/60	98/30/60	98/06/60	98/06/60	98/06/60	10/03/86
FILM	62611	6261J	6261K	6267A	6267B	6267C	6267D	6267E	6267F	6267G	6267H	62671	6267J	6272A	6272B	6272C	6272D	6273A	6273B	6273C	6273D	6273E	6276A

FILM	DATE	SUBSTRATE DESCRIPTION	BEL I TYPE	SOL-GEL ID, (Composition), & AGE in days	COATS & SPIN SPEED	t°C/%RH @ Spln	BAKE PROFILE	SINTER PROFILE	TEL TYPE
6276B	10/03/86	Si Wafer	B29flat	G6251, (8/40/60,+10), 25	10cts @ 2000rpm		¥	550°sinter	~
6276C	10/03/86	Si Wafer	B29rnd	G6251, (8/40/60,+10), 25	10cts @ 2000rpm		NA V	550°sinter	~
6276D	10/03/86	Si Wafer	B29rnd	G6251, (8/40/60,+10), 25	10cts @ 2000rpm		¥	550°sinter	~
6276E	10/03/86	Pt#5	Pt#5	G6251, (8/40/60,+10), 25	10cts @ 2000rpm		¥	550°sinter	~
6279A	10/06/86	Si Wafer	B29flat	G6208, (8/40/60,+10), 71	10cts @ 2000rpm		¥	550°sinter	c
6279B	10/06/86	Si Wafer	B29rnd	G6208, (8/40/60,+10), 71	10cts @ 2000rpm		¥	550°sinter	· ~
6280A	10/07/86	Si Wafer	B29rnd	G6279, (8/40/60,+10), 1	10cts @ 2000rpm		¥	550°sinter	~
6280B	10/07/86	Si 1/4 Wafer	B30-1,LR	G6279, (8/40/60,+10), 1	10cts @ 2000rpm		¥	550°sinter	~
6280C	10/07/86	Si 1/4 Wafer	B30-2,LR	G6279, (8/40/60,+10), 1	10cts @ 2000rpm		¥	550°sinter	~
6280D	10/07/86	Si 1/4 Wafer	B30-3,LR	G6279, (8/40/60,+10), 1	10cts @ 2000rpm		¥	550°sinter	~
6280E	10/07/86	Si 1/4 Wafer	B30-4,LR	G6279, (8/40/60,+10), 1	10cts @ 2000rpm	•	¥	550°sinter	~
6280F	10/07/86	Si 1/4 Wafer	B30-5,LR	G6279, (8/40/60,+10), 1	10cts @ 2000rpm		¥	550°sinter	~
6281A	 10/08/86 Low tem	s : 8/86 Si Wafer Low temp sinter - 500°C.	B29rnd	G6279, (8/40/60,+10), 2	10cts @ 2000rpm		¥	500°sinter	~
6282A	10/09/86 Anneal	Si Wafer 1/4 30min-500°C.	B29rnd 1/4 30min-550	9/86 Si Wafer B29rnd G6279, (8/40/60,+10), 3 Anneal 1/4 30min-500°C, 1/4 30min-550°C:10"/min ramp.	10cts @ 2000rpm		¥	450°sinter	~
6285A	10/13/86	Si 1/4 Wafer	B30-1,LL	G6279, (8/40/60,+10), 6	10cts @ 2000rpm		¥	550°sinter	~
6285B	10/13/86	Si 1/4 Wafer	B30-2,LL	G6279, (8/40/60,+10), 6	10cts @ 2000rpm		¥	550°sinter	~
6285C	10/13/86	Si 1/4 Wafer	B30-3,LL	G6279, (8/40/60,+10), 6	10cts @ 2000rpm		¥	550°sinter	~
6285D	10/13/86	Si 1/4 Wafer	B30-4,LL	G6279, (8/40/60,+10), 6	10cts @ 2000rpm		¥	550°sinter	~
6285E	10/13/86	Si 1/4 Wafer	B30-5,LL	G6279, (8/40/60,+10), 6	10cts @ 2000rpm		Ą	550°sinter	~
6286A	10/14/86	Si 1/4 Wafer	B30-1,UL	G6279, (8/40/60,+10), 7	10cts @ 2000rpm		¥	550°sinter	~
6286B	10/14/86	Si 1/4 Wafer	B30-1,UR	G6279, (8/40/60,+10), 7	10cts @ 2000rpm		Ą	550°sinter	~
6286C	10/14/86	Si 1/4 Wafer	B30-2,UL	G6279, (8/40/60,+10), 7	3cts @ 2000rpm		Ą	550°sinter	6
6286D	10/14/86	Si 1/4 Wafer	B30-2,UR	G6279, (8/40/60,+10), 7	3cts @ 2000rpm		¥.	550°sinter	~

FILM	DATE	SUBSTRATE DESCRIPTION	BEL TYPE	SOL-GEL ID, (Composition), & AGE in days	COATS & SPIN SPEED	t°C/%RH @ Spin	BAKE PROFILE	SINTER PROFILE	TEL
6286E	10/14/86	Si 1/4 Wafer	B30-3,UL	30,+10), 7	10cts @ 2000rpm		¥	550°sinter	٠
6286F	10/14/86	Si 1/4 Wafer	B30-3,UR	G6279, (8/40/60,+10), 7	10cts @ 2000rpm		¥	550°sinter	~
6286G	10/14/86	Si 1/4 Wafer	B30-4,UL	G6279, (8/40/60,+10), 7	3cts @ 2000rpm		¥	550°sinter	~
6286H	10/14/86	Si 1/4 Wafer	B30-4,UR	G6279, (8/40/60,+10), 7	3cts @ 2000rpm		¥	550°sinter	~
62861	10/14/86	Si 1/4 Wafer	B30-5,UL	G6279, (8/40/60,+10), 7	10cts @ 2000rpm		¥	550°sinter	~
6286J	10/14/86	Si 1/4 Wafer	B30-5,UR	G6279, (8/40/60,+10), 7	10cts @ 2000rpm		¥	550°sinter	ć
6286K	10/14/86	Pt#6	9#1d	G6279, (8/40/60,+10), 7	10cts @ 2000rpm		¥	550°sinter	~
6286L	10/14/86	Pt#7	Pt#7	G6279, (8/40/60,+10), 7	10cts @ 2000rpm		ş	550°sinter	č
6287A	10/15/86	Si 1/4 Wafer	B30-3,UR	G6208, (8/40/60,+10), 79	10cts @ 2000rpm		¥	550°sinter	~
6288A	10/16/86	Si 1/4 Wafer	B32-1,LL	G6279, (8/40/60,+10), 9	10cts @ 2000rpm		¥	550°sinter	~
6288B	10/16/86	Si 1/4 Wafer	B32-1,LR	G6279, (8/40/60,+10), 9	10cts @ 2000rpm		¥	550°sinter	~
6288C	 10/16/86	Si 1/4 Wafer	B32-2,LL	G6279, (8/40/60,+10), 9	10cts @ 2000rpm		¥	550°sinter	~
6288D	10/16/86	Si 1/4 Wafer	B32-2,LR	G6279, (8/40/60,+10), 9	10cts @ 2000rpm		¥	550°sinter	<i>د</i>
6288E	10/16/86	Si 1/4 Wafer	B32-3,LL	G6279, (8/40/60,+10), 9	10cts @ 2000rpm		ş	550°sinter	~
6288F	10/16/86	Si 1/4 Wafer	B32-3,LR	G6279, (8/40/60,+10), 9	10cts @ 2000rpm		Ş	550°sinter	٠
6288G	10/16/86	Si 1/4 Wafer	B32-4,LL	G6279, (8/40/60,+10), 9	10cts @ 2000rpm		ş	550°sinter	2
6288H	10/16/86	Si 1/4 Wafer	B32-4,LR	G6279, (8/40/60,+10), 9	10cts @ 2000rpm		ş	550°sinter	~
62881	10/16/86	Si 1/4 Wafer	B32-5,LL	G6279, (8/40/60,+10), 9	10cts @ 2000rpm		ş	550°sinter	٠
6288J	10/16/86	Si 1/4 Wafer	B32-5,LR	G6279, (8/40/60,+10), 9	10cts @ 2000rpm		ş	550°sinter	٠
6293A	10/21/86	Pt#9	Pt#9	G6292, (0/50/50,+10), 1	10cts @ 2000rpm		¥	550°sinter	٠
6293B	10/21/86	Pt#14	Pt#14	G6292, (0/50/50,+10), 1	20cts @ 2000rpm		¥	550°sinter	٠
6293C	10/21/86	Pt#17	Pt#17	G6292, (0/50/50,+10), 1	20cts @ 2000rpm		¥	550°sinter	~
6293D	10/21/86	Si Wafer	Pt on Si	G6292, (0/50/50,+10), 1	5cts @ 2000rpm		Ā	550°sinter	٠

FILM	DATE	SUBSTRATE DESCRIPTION	BEL TYPE	SOL-GEL ID, (Composition), & AGE in days	COATS & SPIN SPEED	t°C/%RH @ Spin	BAKE PROFILE	SINTER PROFILE	TEL TYPE
6294A	10/22/86	Si Wafer	B29rnd	G6292, (0/50/50,+10), 2	7cts @ 2000rpm		¥	550°sinter	٤
6296A	10/24/86	Si Wafer	B35-3/0	G6279, (8/40/60,+10), 17	10cts @ 2000rpm		Ą	550°sinter	~
6296B	10/24/86	Si Wafer	B35-4/0	G6279, (8/40/60,+10), 17	10cts @ 2000rpm		Ą	550°sinter	~
6296C	10/24/86	Si 1/4 Wafer	B35-1,LL	G6279, (8/40/60,+10), 17	10cts @ 2000rpm		N A	550°sinter	~
6296D	10/24/86	Si 1/4 Wafer	B35-2,LL	G6279, (8/40/60,+10), 17	10cts @ 2000rpm		N A	550°sinter	~
6297A	•			G. ().	cts @ rpm				
6297B	·			G. G.	ds @ rpm				
6300A	10/27/86	Si 1/4 Wafer	B33-1	G6292, (0/50/50,+10), 8	10cts @ 2000rpm		Ą	550°sinter	~
6300B	10/27/86	Si 1/4 Wafer	B33-2patt	G6292, (0/50/50,+10), 8	10cts @ 2000rpm		N A	550°sinter	~
63000	10/27/86	Si 1/4 Wafer	B33-3patt	G6292, (0/50/50,+10), 8	8cts @ 2000rpm		N A	550°sinter	٠
6300D	10/27/86	Si 1/4 Wafer	B33-5patt	G6292, (0/50/50,+10), 8	10cts @ 2000rpm	,	Ą	550°sinter	~
6301A	10/28/86	Si Wafer	B34-4	G6300, (8/40/60,+10), 1	10cts @ 2000rpm		¥	550°sinter	~
6301B	10/28/86	Si Wafer	B34-1	G6300, (8/40/60,+10), 1	10cts @ 2000rpm		¥	550°sinter	٠
6301C	10/28/86	Si Wafer	B34-2	G6300, (8/40/60,+10), 1	10cts @ 2000rpm		¥	550°sinter	٠
6301D	10/28/86	Si Wafer	B34-3	G6300, (8/40/60,+10), 1	10cts @ 2000rpm		¥	550°sinter	٠
6301E	10/28/86	Si Wafer	B34-5	G6300, (8/40/60,+10), 1	10cts @ 2000rpm		¥	550°sinter	~
6301F	10/28/86	Si 1/4 Wafer	B35-1,UR	G6300, (8/40/60,+10), 1	10cts @ 2000rpm		ş	550°sinter	~
6301G	10/28/86	Si 1/4 Wafer	B35-1,UL	G6300, (8/40/60,+10), 1	10cts @ 2000rpm		¥	550°sinter	٠
6301H	10/28/86	Si 1/4 Wafer	B32-1,UR	G6279POLY, (8/40/60,+10), 22	10cts @ 2000rpm		Ş	550°sinter	٠
6305A	11/01/86	Si 1/4 Wafer	B35-1,LR	G6300, (8/40/60,+10), 5	10cts @ 2000rpm		¥	550°sinter	~
6305B	11/01/86	Si 1/4 Wafer	B35-2,LR	G6300, (8/40/60,+10), 5	10cts @ 2000rpm		¥	550°sinter	٠
6305C	11/01/86 Oxide	1/86 Si 1/4 Wafer Oxide - No anneal.	B35-3,LL	G6300, (8/40/60,+10), 5	10cts @ 2000rpm		Ā	550°sinter	٠
6305D	11/01/86 Oxide	11/01/86 Si 1/4 Wafer B35-3 Oxide - Annealed - 30min-600°C.	B35-3,UL 500°C	G6300, (8/40/60,+10), 5	10cts @ 2000rpm		N V	550°sinter	~

TEL Type	٥	٠	~	٠	٠	۲	1001	1001	~	٠	٠	٠	٠	٠	٠	• ~	٠	~	<i>د</i>	~	~	<i>~</i>	~
SINTER PROFILE	550°sinter	550°sinter	550°sinter	550°sinter	550°sinter	550°sinter	550°sinter	550°sinter	550°sinter	550°sinter	550°sinter	550°sinter	550°sinter	550°sinter	550°sinter	550°sinter	550°sinter	550°sinter	550°sinter	550°sinter	550°sinter	550 sinter	550 sinter
BAKE PROFILE	Ş	¥	ž	¥	ş	₹	¥	¥	¥	\$	ş	ş	¥	¥	ş	ş	¥	¥	¥	¥	¥	¥	ž
t°C/%RH @ Spin																							
COATS & SPIN SPEED	10cts @ 2000rpm	10cts @ 2000rpm	10cts @ 2000rpm	10ds @ 2000rpm	10cts @ 2000rpm	10cts @ 2000rpm	10cts @ 2000rpm	10cts @ 2000rpm	10cts @ 2000rpm	10cts @ 2000rpm	10cts @ 2000rpm	10cts @ 2000rpm	10cts @ 2000rpm	10cts @ 2000rpm	10cts @ 2000rpm	10cts @ 2000rpm	10cts @ 2000rpm	10cts @ 2000rpm	10cts @ 2000rpm	10cts @ 2000rpm	10cts @ 2000rpm	10cts @ rpm	10cts @ rpm
SOL-GEL ID, (Composition), & AGE in days	30,+10), 5	G6300, (8/40/60,+10), 5	G6300, (8/40/60,+10), 5	G6300, (8/40/60,+10), 5	G6300, (8/40/60,+10), 5	G6300, (8/40/60,+10), 5	G6300, (8/40/60,+10), 9	G6300, (8/40/60,+10), 10	G6307, (15/0/100,+10), 4	G6307, (15/0/100,+10), 4	G6279, (8/40/60,+10), 36	G6279, (8/40/60,+10), 36	G6300, (8/40/60,+10), 24	G6300, (8/40/60,+10), 24	G6300, (8/40/60,+10), 24	G6300, (8/40/60,+10), 24	G6319, (8/40/60,+0), 5	G6319, (8/40/60,+0), 5	G6319, (8/40/60,+0), 5	G6322, (8/0/100,+10), 2	G6322, (8/0/100,+10), 2	G6300, (8/40/60,+10), 32	G6300, (8/40/60,+10), 35
BEL TYPE	æ ·	B35-3,LR	B35-4,LL	B35-4,UL 00°C	B35-4,UR n-600°C	B35-4,LR	~	~	Pt#16	B20	<i>د</i>	~	Pd#2	<i>~</i>	<i>~</i>	~	Pt#1	B38-3,LL	~	Pt#3	B38-3,LR	B39	B40
SUBSTRATE DESCRIPTION	1/86 Si 1/4 Wafer B35-3,U No oxide - Annealed - 30min-600°C.	1/86 Si 1/4 Wafer No oxide - No anneal	1/86 Si 1/4 Wafer Oxide - No anneal	1/86 Si 1/4 Wafer B35-4 Oxide - Annealed - 30min-600°C.	1/86 Si 1/4 Wafer B35-4,Ul No oxide - Annealed - 30min-600°C.	1/86 Si 1/4 Wafer No oxide - No anneal.	OrbTW	OrbTD01cmos	Pt#16	Si Wafer	WTdiO	OrbTD01cmos	Pd#2	~	~	2" Wafer	Pt#1	Si 1/4 Wafer	2" Wafer	Pt#3	Si 1/4 Wafer	8/86 CMOS "Frma": 8/40/60	1/86 CMOS Fred"; 8/40/60.
DATE COATED	11/01/86 No oxid	11/01/86 No oxid	11/01/86 Oxide -	11/01/86 Oxide -	11/01/86 No oxid	11/01/86 No oxid	11/05/86	 11/06/86 "Adeline".	11/07/86	11/07/86	11/13/86	 11/13/86 "Beaulah"	11/20/86	11/20/86	11/20/86	11/20/86	11/20/86	11/20/86	11/20/86	11/20/86	11/20/86	11/28/86 "Frma":	12/01/86 "Fred";
FILM	6305E	6305F	6305G	6305H	63051	6305J	6309A	6310A	6311A	6311B	6315A	6315B	6324A	6324B	6324C	6324D	6324E	6324F	6324G	6324H	63241	6332A	6335A

TEL	6	<i>«</i>	~	~	~	٠	~	~	~	~	~	~	~	~	~	~	٠	٠	~	٠	~	~	~
SINTER PROFILE	550 sinter	550 sinter	550 sinter	550 sinter	550 sinter	550 sinter	550 sinter	550 sinter	550 sinter	550 sinter	550 sinter	550 sinter	550°sinter	550°sinter	30@650inO2	30@650inO2	550°sinter	<i>د</i>	~	<i>د</i>	~	~	~
BAKE PROFILE	NA A	§	¥	¥	¥	¥	¥	¥	¥	ž	ž	¥	ş	¥	2@300	2@300	Ą	2@400	2@400	2@400	2@400	2@400	2@400
t°C/%RH @ Spln																							
COATS & SPIN SPEED	10cts	10cts @ rpm	10cts @ rpm	10cts @ rpm	10cts @ rpm	10cts @ rpm	10cts @ rpm	10cts @ rpm	10cts @ rpm	10cts @ rpm	10cts @ rpm	10cts @ rpm	10cts @ 2000rpm	10cts @ 2000rpm	10cts @ rpm	10cts @ rpm	8cts @ 2000rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	9cts @ rpm
SOL-GEL ID, (Composition), & AGE in days	0,+10),	G6300, (8/40/60,+10), 37	G6300, (8/40/60,+10), 37	G6292, (0/53/47,+10), 47	G6335, (8/40/60,+10), 4	G6335, (8/40/60,+10), 4	G6335, (8/40/60,+10), 4	G6335, (8/40/60,+10), 4	G6335, (8/40/60,+10), 7	G6335, (8/40/60,+10), 7	G6335, (8/40/60,+10), 7	G6335, (8/40/60,+10), 7	G6300, (8/40/60,+10), 50	G6335, (8/40/60,+10), 15	G6292, (0/50/50,+10), 59	G6335, (8/40/60,+10), 16	G6251, (8/40/60,+10), 7	G6292, (0/53/47,+10), 87	G6307, (15/0/100,+10), 72	G6292, (0/53/47,+10), 87	G7006A, (8/40/60,+10), 8	G6307, (15/0/100,+10), 72	G6307, (15/0/100,+10), 73
BEL TYPE	B40	144	841	B41	B4	144	39/40	39/40	39/40	B42	B42	B42	B39,UR	B39,LR	~	~	B25-patt iin ramp	B42	B42	B47-3	B47-3	B47-3	B47-3
SUBSTRATE DESCRIPTION	1/86 CMOS "Ginger": 8/40/60.	CMOS	CMOS	5/86 CMOS "Joc":0/53/47.+10.	CMOS /40/60,+10.	٠	٠	~	CMOS .	CMOS	CMOS	CMOS	Si 1/4 Wafer	Si 1/4 Wafer	Th Oxide	Th Oxide	. : 5/86 Si Wafer B25-pat 30min-600ÅC anneal,10*/min ramp.	A1 .	A2 0,+10.	. A2 +10	A2 +10	A2 0,+10.	5/87 Oxide
DATE	5	12/03/86 "Hector".	12/03/86 "Irene".	12/05/86 "Joc":0/5	12/05/86 CMOS "Kittv": 8/40/60,+10.	12/05/86	12/05/86	12/05/86	· · 12/08/86 "Lerov".	12/08/86 "Mae"	12/08/86 "Nick	12/08/86 "Olga".	12/16/86	12/16/86	12/17/86	12/17/86	 09/15/86 30min-6	01/14/87 0/53/47,+10.	01/14/87 15/0/100,+10	01/14/87 0/53/47,+10.	01/14/87 8/40/60,+10	01/14/87 15/0/100,+10.	01/15/87
	_	_		_		_			_		4.	_	_	_		_		_	_		_	44.5	_

6342B

6342A

6339F

6339E

6339D

6339B

6339A

6335B

6337A

6337B

6342C

6342D

6350A

6350B

6351B

6358E

7014A

7014B

7014C

6351A

7014E

7014D

7015A

FILM	DATE	SUBSTRATE DESCRIPTION	BEL TYPE (SOL-GEL ID, (Composition), & AGE in days	COATS & SPIN SPEED	t°C/%RH Ø Spin	BAKE PROFILE	SINTER PROFILE	TEL
7015B	01/15/87	Oxide	B47-3	G6322, (8/0/100,+10), 58	9cts @ rpm		2@400	Ł	٠
7016A	01/16/87	Oxide	B43	G7006A, (8/40/60,+10), 10	8cts @ rpm		2@400	30@650inO2	~
7016B	01/16/87	Oxide	B43	G7006A, (8/40/60,+10), 10	8cts @ rpm		2@400	30@650inO2	~
7016C	01/16/87	Oxide	B47-5	G6307, (15/0/100,+10), 74	8cts @ rpm		2@400	30@650InO2	٠
7016D	01/16/87	Oxide	B47-4	G6307, (15/0/100,+10), 74	8cts @ rpm		2@400	30@650inO2	~
7021A	01/21/87	Oxide	B47-4	G7006A, (8/40/60,+10), 15	5cts @ rpm		2@400	~	~
7021B	01/21/87	Oxide	B47-4	G7006A, (8/40/60,+10), 15	5cts @ rpm	•	2@400	~	~
7021C	01/21/87	Oxide	B47-4	G7006A, (8/40/60,+10), 15	5cts @ rpm		2@400	٠.	~
7023A	01/23/87	Oxide	B49	G7020, (3/60/40,+10), 3	8cts @ 2000rpm		2@400	30@650inO2	~
7023B	01/23/87	Oxide	B49	G7021, (12/0/100,+10), 2	8cts @ 2000rpm		2@400	30@650inO2	~
7023C	01/23/87	Oxide	B49	G7022, (0/50/50,+10), 1	8cts @ 2000rpm		2@400	30@650inO2	~
7023D	01/23/87	Oxide	B49	G7006A, (8/40/60,+10), 17	8cts @ 2000rpm		2@400	30@650inO2	٠
7023E	01/23/87	Oxide	None	G7021, (12/0/100,+10), 2	8cts @ 2000rpm		2@400	30@650InO2	~
7023F	01/23/87	Oxide	B49	G7006A, (8/40/60,+10), 17	8cts @ 2000rpm		2@450	30@650inO2	~
7023G	01/23/87	Oxide	B49	G7006A, (8/40/60,+10), 17	5cts @ 2000rpm		2@450	30@650inO2	٠
7023H	01/23/87	Oxide	B49	G7006A, (8/40/60,+10), 17	8cts @ 2000rpm		2@450	30@650inO2	~
7028A	01/28/87 15/0/10	8/87 Calde B49 G6307, 315/0/100,+10; Tube#3 settings for 700°C anneal,575,	B49 ngs for 700°C	G6307, (15/0/100,+10), 86 anneal;575,960,665.	8cts @ rpm		2@400	30@700inO2	٠
7028B	01/28/87 8/40/60	8/87 Oxide 8/40/60,+10; 700°C anneal.	. B49	G7006A, (8/40/60,+10), 22	8cts @ rpm		2@400	30@700inO2	٠
7028C	01/28/87 3/60/40	8/87 Oxide 3/60/40,+10; 700°C anneal.		G7020, (3/60/40,+10), 8	8cts @ rpm		2@400	30@700inO2	~
7028D	01/28/87 0/50/50	8/87 Oxide 0/50/50,+10; 700°C anneal.	. B49	G7022, (0/50/50,+10), 6	8cts @ rpm		2@400	30@700inO2	٠
7028E	01/28/87 8/40/60	8/87 Pt#12 PT 8/40/60,+10 on bulk Pt; 700°C anneal.	PŢ °C anneal	G7006A, (8/40/60,+10), 22	8cts @ rpm		2@400	30@700inO2	ГООМ
7030A	01/30/87 Therm	0/87 Th Oxide NONE Thermal oxide on 2"wafer: control for 7030B	NONE control for 703	G6307, (15/0/100,+10), 88 30B.	8cts @ rpm		2@400	30@650inO2	ГОРМ
7030B	01/30/87 Therma	0/87 Th Oxide NONE G630 Thermal oxide on 2"wafer; first composite FES on oxide.	NONE irst composite	G6307/7006A, FES on oxide.	2/6cts @ rpm		2@400	30@650inO2	ГОДМ

FILM	DATE	SUBSTRATE DESCRIPTION	BEL TYPE	SOL-GEL ID, Composition), & AGE in days	COATS & SPIN SPEED	t°C/%RH @ Spin	BAKE PROFILE	SINTER PROFILE	TEL
7030C	01/30/87 thermal	0/87 Th Oxide NONE thermal oxide on 2"wafer; controlfor 7030B.	NONE controlfor 7030	G7006A, (8/40/60,+10), 24)B	8cts @ rpm		2@400	30@650inO2	LODM
7030D	01/30/87 Anneale	0/87 Th Oxide B	B49 lion	G7006A, (8/40/60,+10), 24	8cts @ rpm		2@400	30@650inO2	LODM
7035A	02/04/87 Etched	4/87 Th Oxide NONE Etched paddles - annealed 1/2 of wafer.	NONE 1/2 of wafer.	G6307/7006A,	1/7cts @ rpm		2@400	30@650inO2	LODM
7035B	02/04/87 Etched	4/87 Th Oxide NONE Etched paddles - annealed 1/2 of wafer.	NONE 1/2 of wafer.	G6307/7022,	1/7cts @ rpm		2@400	30@650inO2	LODM
7035C	02/04/87 Etched	4/87 Th Oxide NONE Etched paddles - annealed 1/2 of wafer.	NONE 1/2 of wafer.	G6307/7020,	1/7cts @ rpm		2@400	30@650inO2	LODM
7035D	02/04/87 Etched	4/87 Si Wafer NONE Etched paddles - annealed 1/2 of wafer.	NONE 1/2 of wafer.	G6307, (15/0/100,+10), 93	8cts @ rpm		2@400	30@650inO2	LODM
7036A	02/05/87 1*LODA	5/87 Si Wafer B50-4 1*LODM; composite FES - 8/40/60 over 15/0/100.	B50-4 8/40/60 over	G6307/7006A, 15/0/100.	1/7cts @ rpm		2@400	30@650inO2	LODM
7036B	02/05/87 1*LODA	5/87 Si Wafer B50-4 1*LODM; composite FES - 3/60/40 over 15/0/100.	B50-4 3/60/40 over	G6307/7020, 15/0/100.	1/7ⴛა @ იხო		2@400	30@650inO2	FODM
7036C	02/05/87 1"LODA	5/87 Si Wafer B50-4 1*LODM; composite FES - 0/50/50 over 15/0/100.	B50-4 0/50/50 over	G6307/7022, 15/0/100.	1/7ds @ ന്റന		2@400	30@650inO2	FODM
7036D	02/05/87 Etched	5/87 Si Wafer NONE Etched paddles - annealed 1/2 of wafer.	NONE 1/2 of wafer.		1/7ds @ ppm		2@400	30@650inO2	LODM
7036E	02/05/87 Control	5/87 Si Wafer Control for 7036A-D.	NONE	G7006A, (8/40/60,+10), 30	8cts @ rpm	•	2@400	30@650inO2	FODM
7037A	02/06/87 1000Å	6/87 1000Å П очег spin on oxide.	NONE 9	G6307/7006A,	1/7cts @ rpm		2@400	30@650inO2	LODM
7037B	02/06/87 Ti remo	6/87 Oxide SpOn N Ti removed from spin on oxide.	NONE ide	G6307/7006A,	1/7cts @ rpm		2@400	30@650inO2	LODM
7037C	02/06/87 Ti thinn	500Å TI led to about 500Å, th	NONE ninner toward	6/87 500Å TI NONE G6307/7006Å, Ti thinned to about 500Å, thinner toward edge;spin on oxide.	1/7ds @ ppm		2@400	30@650inO2	FODM
7037D	02/06/87 FES on	6/87 1000A TI FES on spin on oxide control.	NONE ol	G7006A, (8/40/60,+10), 31	8cts @ rpm		2@400	30@650inO2	LODM
7037E	02/06/87 1/4-Orb	6/87 OxideORBTW NONE 1/4-Orbit TW with 209 oxide over nitride.	NONE e over nitride.	G6307/7006A,	1/7cts @ rpm		2@400	попе	FODM (
7037F	02/06/87 1/4-Orb	6/87 OxideORBTW NONE 1/4-Orbit TW with 209 oxide over nitride; HF dip.	NONE e over nitride;	G6307/7006A, HF dip	1/7cts @ rpm		2@400	none	FODM
7037G	02/06/87 1/4-Orb	6/87 OxideORBTW NONE 1/4-Orbit TW with 2 coats 209 oxide.	NONE 209 oxide.	G6307/7006A,	1/7ds @ ppm		2@400	ноп	MGOT
7038A	02/07/87 1/4-Orb	7/87 Orbit TW NONE 1/4-Orbit TW with 2 coats 209 oxide.	NONE 209 oxide.	G7006A, (8/40/60,+10), 32	8cts @ rpm		2@400	өиои	LODM
7038B	02/07/87 1/4-Orb	7/87 Orbit TW NONE 1/4-Orbit TW with 2 coats 209 oxide.	NONE 209 oxide.	G7006A, (8/40/60,+10), 32	8cts @ rpm		2@400	none	MOOT
7040A	02/09/87 1/4-Orb	9/87 Orbit TW NONE 1/4-Orbit TW with 2 coats 209 oxide.	NONE 209 oxide.	G7006A, (8/40/60,+10), 34	8cts @ rpm		2@400	none	LODM
7040B	02/09/87 1/4-Orb	9/87 Orbit TW NONE 1/4-Orbit TW with 2 coats 209 oxide.	NONE 209 oxide.	G7006A, (8/40/60,+10), 34	8cts @ rpm		2@400	none	LODM
7042A	02/11/87 Thin Ti.	Orbit TW	NONE	G7006A, (8/40/60,+10), 36	8cts @ rpm		2@400	30@650inO2	MGOT

TEL TYPE	LODM	LODM	MOOT	MOOT	MOOT	MOOT	MGOT	MQOI	nt S	Fut S	Int S	nt S	Int S	Int S	Ints	MOOT	MOOT	MOOT	LODM	LODM	MOOT	LODM	MOOT
FÀ	9	2	2	9	9	9	9	9	<u>_</u>	두	-	_	<u> </u>	드	드	2	2	2	2	2	2	2	2
SINTER	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	in A r30@650	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2
SIP	30@6	30@	30@	30@	30@	30@	30 80 80 80 80 80 80 80 80 80 80 80 80 80	30	300	30	30@	30@	30@	30@	30@	inAr	30@	30@	30@	30@	30@	30@	30@
BAKE	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400
	×	ส	ส	ิ	ă	ิ	ิ	ิ	ิ	ิส	ิ	ิ	ิ	ิ	ิ	ิ	ิ	ิ	ผี	ิ	Ñ	Ñ	ณ <u>ี</u>
t°C/%RH																							
R SPIN	rpm	mdı	md ₁	md.	md.	md.	md.	md.	md.	md.	md.	md.	rpm	md.	md.	rpm 	md.	rpm c	md .	ndu (ndı (rpm	md.
COATS & SPIN	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm
	1	36	37	37	38	38	38	38	38	38	38	38 8	38	38	38	42	-	-	_	-	-	-	_
SOL-GEL ID,	G7006A, (8/40/60,+10), 36	(8/40/60,+10), 36	(8/40/60,+10), 37	G7006A, (8/40/60,+10), 37	(8/40/60,+10), 38	G7006A, (8/40/60,+10), 38	G7006A, (8/40/60,+10), 38	(8/40/60,+10), 38	G7006A, (8/40/60,+10), 38	(8/40/60,+10), 38	(8/40/60,+10), 38	(8/40/60,+10), 38	(8/40/60,+10), 38	(8/40/60,+10), 38	(8/40/60,+10), 38	G7006A, (8/40/60,+10), 42	G7055, (8/40/60,+10),	G7055, (8/40/60,+10), 1	(8/40/60,+10),	(8/40/60,+10),	(8/40/60,+10), 1	(8/40/60,+10),	(8/40/60,+10), 1
SOL-G	6A, (8/40		6A, (8/40	6A, (8/40	16A, (8/4C	16A, (8/40	16A, (8/40	16A, (8/40	16A, (8/40	16A, (8/40)6A, (8/40)6A, (8/40)6A, (8/40)6A, (8/40)6A, (8/4()6A, (8/40)55, (8/4 <u>(</u>	355, (8/4 ₍	G7055, (8/40	G7055, (8/40	G7055, (8/40	G7055, (8/4(_
Compos	G700	G7006A,	G7006A,	C700	G7006A,	G700	C700	G7006A,	G700	G7006A,	G7006A,	G7006A,	G7006A,	G7006A,	G7006A,	G700	. 62	G7(nneal	G7	G7			G7 diate ann
BEL	1	NONE	NONE	NONE	B49	B54-1	B54-2	B54-3	B54-1 ·1A etch	B54-2 -2A etch	B54-3	B54-1 -1B etch	B54-2 -2B etch	B54-3	B54-3	B49	56-5 oat/bake.	5/87 Oxide OrbTW 56-5 Same as 7056A-9 but H2NO3 dip atter anneal.	56-5 t/bake	56-5 anneal.	5/87 Oxide OrbTW 56-5 Immediate anneal then R10 treatment X2.	5/87 Oxide OrbTW 56-5 Simulate CMOS R10; immediate anneal.	5/87 Oxide OrbTW 56-5 G7055, Simulate CMOS with acetone/IPA; immediate anneal.
		Z		Z		•	•	•	B at; B54-1	B et; B54-2		B et; B54-1	B et; B54-2				W √after ∞	W .	W after coat	W mediate	W R10 tre	W immedia	W acetone/
SUBSTRATE	Orbit TW	Orbit TW	OxideORBTW	CMOS	3/87 CMOS Standard BEL; 1*LODM.	3/87 Oxide 250Å Ti/1500Å Pt;1"LODM.	3/87 Oxide 500Å Ti/750Å Pt; 1"LODM.	3/87 Oxide 500Å Ti/500Å Pt; 1"LODM.	3/87 Oxide B54-1 1/4-4 wafer; paddle set; B54-1A etch.	3/87 Oxide B54-2 1/4-4"wafer; paddle set; B54-2A etch.	3/87 Oxide 1/4-4"wafer; paddle set.	3/87 Oxide B54-1 1/4-4"wafer; paddle set; B54-1B etch.	3/87 Oxide B54-2 1/4-4*wafer; paddle set; B54-2B etch.	3/87 Oxide 1/4-4"wafer; paddle set.	3/87 CMOS 1/4-4"wafer; paddle set.	CMOS gon	5/87 Oxide OrbTW 56-5 Annealed immediately after coat/bake.	Oxide OrbTW 056A-9 but H2	5/87 Oxide OrbTW 56-5 Annealed ~72 hours after coat/bake.	5/87 Oxide OrbTW 56-5 R10 treatment then immediate anneal.	Oxide OrbTW	Oxide OrbTW MOS R10; im	xide OrbT
	⊨	≓	≓	2/87 Thin Ti	r ndard BE	, Å Tiv150	, A Ti/750,	, A Ti/500,	4"wafer;	7 4"wafer;	7 4"wafer;	4"wafer;	7 -4"wafer;	7 4"wafer;	7 -4"wafer;	7/87 CM Anneal in Argon.	7 nealed in	7 ne as 70	7 nealed ~7	7 O	7 O nediate a	7 oulate CA	7 oulate Ch
DATE	02/11/87 Thin Ti.	02/11/87 Thin Ti.	02/12/87 Thin	02/12/87 Thin	02/13/87 Star	02/13/87 250/	02/13/87 500	02/13/87 500,	02/13/87	02/13/87 1/4~	02/13/87 1/4~	02/13/87	02/13/87 1/4-	02/13/87	02/13/87 1/4~	02/17/87 Ann	02/2	7056A-1 02/25/87 Sam	7056A-2 02/25/87 Ann	7056A-3 02/25/87 R10	7056A-4 02/25/87	7056A-5 02/25/87 Sim	7056A-6 02/25/87 Sim
E C	7042B	7042C	7043A	7043B	7044A	7044B	7044C	7044D	7044E	7044F	7044G	7044H	70441	7044J	7044K	7048A	7056A-1	7056A-1	7056A-2	7056A-3	7056A-4	7056A-5	7056A-(
	18	-	•	-	•	-	-																

		z	BEL	SOL-GEL ID, (Composition), & AGE in days	00	t°C/%RH @ Spin	BAKE PROFILE	PROFILE	TYPE
7056A-7	02/2	5/87 Oxide OrbTW 56-5 Simulate CMOS with 130; immediate anneal	56-5 nmediate a	G7055, 	8cts @ rpm		2@400	30@650inO2	MOO
7056A-8 02/25/87 Spin	02/25/87 Spin on	5/87 Oxide OrbTW 56 Spin on PT; immediate anneal	56-5 al	G7055, (8/40/60,+10), 1	8cts @ rpm		2@400	30@650inO2	FODW
7056A-9 02/25/87 Ann	02/25/87 Anneald	Oxide OrbTW led 72 hours after coa	56-5 at/bake but	5/87 Oxide OrbTW 56-5 G7055, (8/40/60,+10), 1 Annealed 72 hours after coat/bake but bake prior to anneal.	8cts @ rpm		2@400	30@650inO2	M OO1
7059A	02/28/87 New so	8/87 Oxide OrbTW B50-4 New sol-gel test;suspect IPA(Alfa).	B50-4 A(Alfa).	G7047, (8/40/60,+10), 12	8cts @ rpm		2@400	30@650inO2	FODM
7059B	02/28/87 Control	8/87 Oxide OrbTW Control for 7059A	B50-4	G7055, (8/40/60,+10), 4	8cts @ rpm		2@400	30@650inO2	MGOT
7069A	03/10/87 Ox Imm. anneal.	Oxide OrbTW	B57-2	G7055, (8/40/60,+10), 14	8cts @ rpm		2@400	30@650inO2	Fat1
7069B	03/10/87 Ox Imm. anneal.	Oxide OrbTW	B57-3	G7055, (8/40/60,+10), 14	8cts @ rpm		2@400	30@650inO2	Fat1
7069C	03/10/87 Oxi	Oxide OrbTW	B57-4	G7055, (8/40/60,+10), 14	8cts @ rpm		2@400	30@650inO2	Fat1
7069D	03/10/87 Ox Imm. anneal.	Oxide OrbTW nneal.	B57-5	G7055, (8/40/60,+10), 14	8cts @ rpm		2@400	30@650inO2	Fat1
7075A	03/16/87 Ox Imm. anneal.	Oxide OrbTW nneal.	B60-1	G7055, (8/40/60,+10), 20	8cts @ rpm		2@400	30@650inO2	Fat1
7075B	03/16/87 Oy Imm. anneal	Oxide OrbTW Inneal.	B60-2	G7055, (8/40/60,+10), 20	8cts @ rpm		2@400	30@650inO2	Fat1
7075C	03/16/87 ASM at	6/87 ASM32 ASM aligner test	B60-2	G7047, (8/40/60,+10), 28	8cts @ rpm		2@400	9000	Fat1
7075D	03/16/87 ASM al	6/87 ASM33 ASM aligner test.	B60-2	G7047, (8/40/60,+10), 28	8cts @ rpm		2@400	9000	Fat1
7075E	03/16/87 ASM al	6/87 ASM35 ASM35 ASM aligner test.	B60-2	G7047, (8/40/60,+10), 28	8cts @ rpm		2@400	30@650inO2	Fat1
7076A	03/17/87 3/40/60	7/87 ? 3/40/60,+10;imm.anneal	B62-1	G7072, (3/40/60,+10), 4	8cts @ rpm		2@400	30@650inO2	Fat1
7076B	03/17/87 0/50/50	7/87 ? 0/50/50,+10;imm.anneal	B62-2	G7022, (0/50/50,+10), 54	8cts @ rpm		2@400	30@650inO2	Fat1
7076C	03/17/87 15/0/10	7/87 15/0/100,+10;imm.anneal.	B62-4	G7068, (15/0/100,+10), 8	8cts @ rpm		2@400	30@650inO2	Fat1
7077A	03/18/87 Diana's	8/87 Diana's 1st;0/50/50	B61-2	G7022, (0/50/50,+10), 55	8cts @ rpm		2@400	30@650inO2	ГОРМ
7077B	03/16/87 Diana's	6/87 Diana's 1st;3/40/60	B61-2	G7072, (3/40/60,+10), 5	8cts @ rpm		2@400	30@650inO2	ГОРМ
7077C	03/18/87 Diana's	9/87	B61-2	G7020, (3/60/40,+10), 57	8cts @ rpm		2@400	30@650inO2	MOOT
7077D	03/18/87 Diana's	8/87 Diana's 1st;8/40/60.	B61-2	G7047, (8/40/60,+10), 30	8cts @ rpm		2@400	30@650inO2	FODM
7077E	03/18/87 Diana's	8/87 Si Wafer NONE Si Wafer Diana's 1st;composite test, 15/0/100 under 8/40/60.	NONE 15/0/100	G7068/7047, under 8/40/60	1/7cts @ rpm		2@400	30@650inO2	MOOT
7077F	03/18/87 Diana's	8/87 Th Oxide NONE Diana's 1st;composite test, 15/0/100 under 8/40/60.	NONE 15/0/100	G7068/7047, under 8/40/60.	1/7cts @ rpm		2@400	30@650inO2	MOOT

TEL	МООЛ	FODM	ГОРМ	MOOT	FODM	MOOT	Fat1	Fatt	Fat1	Fat1	Fat1	Fat1	FODM	FODM	FODM	Fat1	Fat1	Fat1	Fat1	Fat1	Fat1	Fat1	ì
SINTER	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	
BAKE	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	
t°C/%RH @ Spin																							
COATS & SPIN	8ds (8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	,
SOL-GEL ID,	, (8/40/60,+10), 27	G7055, (8/40/60,+10), 27 under 8/40/60.	G7055, (8/40/60,+10), 27 under 8/40/60.	G7055, (8/40/60,+10), 27 der 8/40/60.	G7055, (8/40/60,+10), 27 der 8/40/60.	G7055, (8/40/60,+10), 27 der 8/40/60.	G7047, (8/40/60,+10), 38 der 8/40/60.	G7047, (8/40/60,+10), 38 der 8/40/60.	G7047, (8/40/60,+10), 38 der 8/40/60.	G7047, (8/40/60,+10), 38 der 8/40/60.	GGB7085, (3/40/60,+10), 18/64 7068 giving a 3/40/60,+10	G7055, (8/40/60,+10), 34	G7055, (8/40/60,+10), 34 Jdy; 7089B-1 thru 8.	G7047, (8/40/60,+10), 46 Jdy; 7089B-1 thru 8.	G7047, (8/40/60,+10), 46 Jdy; 7089B-1 thru 8.	G7047, (8/40/60,+10), 47	G7047, (8/40/60,+10), 47 std. anneal	4/87 Th Oxide B61-4 G7047, (8/40/60,+10), 47 Scratch protection study; 2in/min ramp-in/out,30"@650°anneal.	4/87 Th Oxide B61-5 G7047, (8/40/60,+10), 47 Scratch protection study: fast rame-in/out 30*@650*anneal	G7047, (8/40/60,+10), 47	G7047, (8/40/60,+10), 47	G7047, (8/40/60,+10), 47 std. anneal.	
BEL	Š	B64-1 15/0/100 und	B56-3 15/0/100 und	B64-2 G7055 15/0/100 under 8/40/60.	B64-3 15/0/100 und	B64-4 G7055 15/0/100 under 8/40/60.	B65-2 15/0/100 und	B65-3 15/0/100 und	B65-4 15/0/100 und	B65-5 15/0/100 und	B65-1 7022 and G7	B63-1 in field.	B66-1 EL barrier stu	B66-1 EL barrier stu	B66-1 EL barrier stu	B61-1 andard anne	B61-3 3 hrs before a	B61-4 n/min ramp-i	B61-5 st ramo-in/o	B62-5 8 hrs before	B63-2	B63-3 8 hrs before	
SUBSTRATE	3/87 Orbit TW Diana's 1st;composite test.	3/87 Orbit TW Diana's 1st;composite test,	3/87 CMOS Diana's 1st;composite test,	3/87 Orbit TW Diana's 1st;composite test,	3/87 Orbit TW B64-3 G7055 Diana's 1st; composite test, 15/0/100 under 8/40/60.	3/87 Orbit TW Diana's 1st;composite test,	6/87 Th Oxide B65-2 G7047 Diana's 1st; composite test, 15/0/100 under 8/40/60.	6/87 Th Oxide B65-3 G7047 Diana's 1st;composite test, 15/0/100 under 8/40/60.	6/87 Th Oxide B65-4 G7047 Diana's 1st; composite test, 15/0/100 under 8/40/60.	6/87 Th Oxide B65-5 G7047 Diana's 1st;composite test, 15/0/100 under 8/40/60.	7/87 Th Oxide B65-1 GGB7085, GB7085 is 80/20 blend of G7022 and G7068 giving a	0/87 Th Oxide B63-1 6000Å oxide/TiO2/Pt; no Ti in field.	0/87 Th Oxide B66-1 G7055, Sectioned for 1" LODM's; TEL barrier study; 7089B-1	3/87 ASM F>B B66-1 G7047, Sectioned for 1" LODM's; TEL barrier study; 7089B-1	3/87 ASM F>B B66-1 G7047, Sectioned for 1" LODM's; TEL barrier study; 7089B-1	4/87 Th Oxide B61-1 Scratch protection study; standard anneal.	4/87 Th Oxide B61-3 G7047 Scratch protection study; 48 hrs before std. anneal.	Th Oxide protection study; 2i	Th Oxide protection study: fa	4/87 Th Oxide B62-5 Scratch protection study: 48 hrs before std.	4/87 Th Oxide B63-2 Scratch protection study: standard anneal.	4/87 Th Oxide B63-3 G7047 Scratch protection study: 48 hrs before std. anneal.	
DATE	03/23/87 Diana's	03/23/87 Diana's	03/23/87 Diana's	03/23/87 Diana's	03/23/87 Diana's	03/23/87 Diana's	03/26/87 Diana's	03/26/87 Diana's	03/26/87 Diana's	03/26/87 Diana's	03/27/87 GB7085	03/30/87 6000Å c	03/30/87 Section	04/03/87 Section	04/03/87 Section	04/04/87 Scratch	04/04/87 Scratch	04/04/87 Scratch	04/04/87 Scratch	04/04/87 Scratch	04/04/87 Scratch	04/04/87 Scratch	
FILM	7082A	7082B	7082C	7082D	7082E	7082F	7085B	7085C	7085D	7085E	7086A	7089A	7089B	7093A	7093B	7094A	7094B	7094C	7094D	7094E	7094F	7094G	

FILM	DATE COATED	SUBSTRATE DESCRIPTION	BEL TYPE	SOL-GEL ID, (Composition), & AGE in days	COATS & SPIN	t°C/%RH @ Spin	BAKE PROFILE	SINTER PROFILE	TEL
70941	04/04/87 Scratch	Th Oxide protection study; fa	B63-5 ast ramp-in/c	ᇹᇃ	8cts @ rpm		2@400	30@650inO2	Fatt
7094J	04/04/87 Scratch	4/87 Th Oxide B66-2 G7047 Scratch protection study; 48 hrs before std. anneal.	B66-2 18 hrs before	G7047, (8/40/60,+10), 47 std. anneal.	8cts @ rpm		2@400	30@650inO2	Fat1
7094K	04/04/87 Scratch	4/87 Th Oxide B66-3 G7047 Scratch protection study; 48 hrs before std. anneal.	B66-3 18 hrs before	. •	8cts @ rpm		2@400	30@650inO2	Fat1
7094L	04/04/87 Scratch	4/87 Th Oxide B67-1 G7047, Scratch protection study;FES lifting in field at dep. ct.	B67-1 ES lifting in f	G7047, (8/40/60,+10), 47 lield at dep. ct.8.	8cts @ rpm		2@400	30@650inO2	Fat1
7096A	04/06/87 2000rp	6/87 Th Oxide B50-4 G7090B 2000rpm spin, DEKTAK; crazing by 4th ∞ at; stopped	B50-4 razing by 4th	G7090B, (8/40/60,+30*), 6 oat; stopped coating	5cts @ rpm		2@400	30@650inO2	Fat1
7096B	04/06/87 4000rp	6/87 Th Oxide 4000rpm spin, DEKTAK.	B50-4		5cts @ rpm		2@400	30@650inO2	Fat1
7096C	04/06/87 Excess	6/87 Th Oxide Excess Pb study.	B66-4	G7090A, (8/40/60,+0), 6	8cts @ rpm		2@400	30@650inO2	MOOT
7096D	04/06/87 Excess	6/87 Th Oxide Excess Pb study	B66-4	G7091, (8/40/60,+30), 5	8ds @ rpm		2@400	30@650inO2	FODM
7096E	04/06/87 New ∝	6/87 Th Oxide New composition.	B66-4	G7092, (6/50/50,+10), 4	8cts @ rpm		2@400	30@650inO2	rod _M
7096F	04/06/87 Fast ra	5/87 Th Oxide Fast ramp study.	B66-4	G7047, (8/40/60,+10), 49	8cts @ rpm		2@400	MufFur650	MOOT
7096G	04/06/87 Slow re	6/87 Th Oxide Slow ramp study.	B66-4	G7047, (8/40/60,+10), 49	8cts @ rpm		2@400	2"/-650°	FODM
7096H	04/06/87 Contro	6/87 Th Oxide Control for 70961.	B66-4	G7072, (3/40/60,+10), 24	8cts @ rpm		2@400	30@650inO2	W OO1
19607	04/06/87 Blende	6/87 Th Oxide Blended Gel	B66-4	GB7085, (3/40/60,+10), 28/74	8cts @ rpm		2@400	30@650inO2	LODM
10967	04/06/87 2X std.	Th Oxide sol-gel concentration	B66-4 on; stopped	6/87 Th Oxide B66-4 G7090B, (8/40/60,+30*), 6 2X std. sol-gel concentration; stopped at 4th coat; annealed.	4cts @ rpm		2@400	30@650inO2	M GO1
7097A	04/07/87 2X std.	7/87 Th Oxide B66-4 G7090B, (8/ 2X std. sol-gel concentration; spin 4 coats at 4000 rpm.	B66-4 on; spin 4 co	G7090B, (8/40/60,+30*), 7 ats at 4000 rpm	4cts @ rpm		2@400	30@650inO2	FODM
7097B	04/07/87 Pre 51	7/87 Orbit TW Pre 512 process tune-up.	B70-3	G7047, (8/40/60,+10), 50	8cts @ rpm		2@400	30@650inO2	1001
7097C	04/07/87 Pre 51	7/87 Orbit TW Pre 512 process tune-up.	B71-3	G7047, (8/40/60,+10), 50	8cts @ rpm		2@400	30@650inO2	<u>1</u> 00
7097D	04/07/87 Pre 51	7/87 CMOS Pre 512 process tune-up.	B71-4	G7047, (8/40/60,+10), 50	8cts @ rpm		2@400	30@650inO2	<u>1</u> 00
7097E	04/07/87 Pre 51	7/87 Orbit TW Pre 512 process tune-up.	B70-1	G7047, (8/40/60,+10), 50	8cts @ rpm		2@400	30@650inO2	<u>6</u>
7097F	04/07/87 Pre 51	7/87 CMOS Pre 512 process tune-up.	B71-5	G7047, (8/40/60,+10), 50	8cts @ rpm		2@400	30@650inO2	<u>Б</u>
7098A	04/08/87 24 coa	8/87 Th Oxide B66-5 24 coats (3x8), anneal after each 8 cfs.	B66-5 er each 8 cts.	G7047, (8/40/60,+10), 51 . For Dr.McInerney	24cts @ rpm		2@400	30@650inO2	1 00
7098B	04/08/87 24 coa	8/87 Th Oxide B66-5 24 coats (3x8), anneal after each 8 cts.	B66-5 ar each 8 cts.	G7047, (8/40/60,+10), 51 . For Dr.Land	24cts @ rpm		2@400	30@650inO2	<u></u>
7098C	04/08/87 24 coa	8/87 Th Oxide B66-5 24 coats (3x8), anneal after each 8 cts.	B66-5 er each 8 cts	G7020, (3/60/40,+10), 78 . For Dr.McInerney	24cts @ rpm		2@400	30@650inO2	100t

	DATE COATED	E O	BEL TYPE	SOL-GEL ID, (Composition), & AGE in days	8	t°C/%RH @ Spin	BAKE PROFILE	SINTER	TEL
7098D	04/08/87 24 coat	8/87 Th Oxide B66-5 24 coats (3x8), anneal after each 8 cts.	B66-5 each 8 cts.	G7020, (3/60/40,+10), 78 For Dr.Land	24cts @ rpm		2@400	30@650inO2	<u></u>
7098E	04/08/87 ECD51	8/87 TW ECD512 ECD512 test wafer.	B73-2	G7047, (8/40/60,+10), 51	8cts @ rpm		2@400	30@650inO2	512
7098F	04/08/87 ECD51;	8/87 TW ECD512 ECD512 test wafer.	B73-3	G7047, (8/40/60,+10), 51	8cts @ rpm		2@400	30@650inO2	512
7098G	04/08/87 Multiple	8/87 Th Oxide B66-5 Multiples of 8 coats, anneal after each 8 cts.	B66-5 after each 8	G7047, (8/40/60,+10), 51 cts	32cts @ rpm		2@400	30@650inO2	512
7099A	04/09/87 FES ov	Nitride rer single layer spin-or	B66-5 n Ti900(oxid	9/87 Nitride B66-5 G7047, (8/40/60,+10), 52 FES over single layer spin-on Ti900(oxidized @ 650 for 30 min).	8cts @ rpm		2@400	30@650InO2	512
7100A	04/10/87 FES ov	0/87 Nitride B66-5 G7047, FES over two layers spin-on Ti900(oxidized @ 650 for	B66-5 T1900(oxidiz	G7047, (8/40/60,+10), 53 zed @ 650 for 30 min)	8cts @ rpm		2@400	30@650inO2	512
7100B	04/10/87 FES ov	0/87 Nitride B66-5 G7047, FES over two layers spin-on Ti900(oxidized @ 750 for	B66-5 Ti900(oxidiz	G7047, (8/40/60,+10), 53 2ed @ 750 for 30 min)	8cts @ rpm		2@400	30@650inO2	512
7104A	04/14/87 FES ov	4/87 CMOS B75-1 FES over two layers spin-on Ti900(oxidized	B75-1 T1900(oxidiz	G7055, (8/40/60,+10), 49 zed @ 750 for 30 min)	8cts @ rpm		2@400	30@650inO2	1001
7104B	04/14/87 FES ov	4/87 CMOS B75-2 FES over two layers spin-on Ti900(oxidized	B75-2 T1900(oxidiz	G7055, (8/40/60,+10), 49 zed @ 750 for 30 min)	8cts @ rpm		2@400	30@650inO2	100 <u>1</u>
7104C	04/14/87 ECD51	4/87 TW ECD512 ECD512 test wafer	B74-2	G7055, (8/40/60,+10), 49	8cts @ rpm		2@400	30@650inO2	512
7104D	04/14/87 ECD51	4/87 TW ECD512 ECD512 test wafer.	B74-3	G7055, (8/40/60,+10), 49	8cts @ rpm		2@400	30@650inO2	515
7105A	04/15/87 ECD51:	5/87 TW ECD512 ECD512 test wafer.	B76-1	G7055, (8/40/60,+10), 50	8cts @ rpm		2@400	30@590inO2	512
7105B	04/15/87 ECD51:	5/87 TW ECD512 ECD512 test wafer.	B76-2	G7055, (8/40/60,+10), 50	8cts @ rpm		2@400	30@650inO2	512
7105C	04/15/87 CMOS	5/87 ECD512A CMOS ECD512A	B76-3	G7055, (8/40/60,+10), 50	8cts @ rpm		2@400	30@650inO2	512
7105D	04/15/87 CMOS	5/87 ECD512A CMOS ECD512A.	B76-4	G7055, (8/40/60,+10), 50	8cts @ rpm		2@400	30@590inO2	512
7106A	04/16/87 Control	6/87 Th Oxide Control for 7106 film series.	B56-3	G7072, (3/40/60,+10), 34	8cts @ rpm		2@400	30@650inO2	MOOT
7106B	04/16/87 GB708	6/87 Th Oxide B56-3 GB7085, GB7085 is 80/20 blend of G7022 and G7068 giving a \$	B56-3 7022 and G7	GB7085, (3/40/60,+10), 21 7068 giving a 3/40/60,+10	8cts @ rpm		2@400	30@650inO2	MOOT
7106C	04/16/87 GB710	6/87 Th Oxide B56-3 GB7106A is 50/50 blend of G7072 &	B56-3 37072 & G7	GB7106A, (5.5/40/60,+5), <1 G7090A; 5.5/40/60,+5.	8cts @ rpm		2@400	30@650inO2	MOOT
7106D	04/16/87 GB710	6/87 Th Oxide B56-3 GB7106B is 50/50 blend of G7072 &	B56-3 G7072 & G7	GB7106B, (5.5/40/60,+10), <1 G7055; 5.5/40/60,+10	8cts @ rpm		2@400	30@650inO2	MGOT
7106E	04/16/87 GB710	Th Oxide 36C is 1/2:1/6:1/3 blen	B56-3 nd of G7072	6/87 Th Oxide B56-3 GB7106C, (5.5/40/60,+15), <1 GB7106C is 1/2:1/6:1/3 blend of G7072:7090A:7091;5.5/40/60,+15.	8cts @ rpm		2@400	30@650inO2	ГОРМ
7106F	04/16/87 GB710	6/87 Th Oxide B56-3 GB7106D, (8 GB7106D is 5/6:1/6 blend of G7090A & 7091; 8/40/60,+5.	B56-3 I G7090A &	GB7106D, (8/40/60,+5), <1 7091; 8/40/60,+5.	8cts @ rpm		2@400	30@650inO2	W OO1
7106G	04/16/87 GB710	Th Oxide IGE is 50:50 blend of (B56-3 37090A & 7	6/87 Th Oxide B56-3 GB7106E, (8/40/60,+15), <1 GB7106E is 50:50 blend of G7090A & 7091; 8/40/60,+15.	8cts @ rpm		2@400	30@650inO2	FODM
7106H	04/16/87 Control	6/87 Th Oxide Control for 7106 film series.	B56-3	G7055, (8/40/60,+10), 51	8cts @ rpm		2@400	30@650inO2	LODM

FILM DATE SUBSTRATE IN COATED DESCRIPTION T	7114A 04/24/87 Nit+TiO2 550Å TiO2 under BEL study; 5	7114B 04/24/87 Nit+TiO2 750Å TiO2 under BEL study; 5	7114C 04/24/87 Nit+TiO2 1050Å TiO2 under BEL study;	7114D 04/24/87 Nitride B7/ Nitride under 850Å TI/1000Å Pt.	7114E 04/24/87 Th Oxide B7 Oxide under 850A Ti/1000A Pt.	7114F 04/24/87 Th Oxide B68-3 Spin-on oxide/interlevel dielectric study.	7114G 04/24/87 Th Oxide B68-4 G7110, Spin-on oxide/interlevel dielectric study;FES litting @	7114H 04/24/87 Th Oxide B68-5 G7110, Spin-on oxide/interlevel dielectric study;FES lifting @	7117A 04/27/87 TD01 CMOS B77-5 TD01 CMOS with nitride removed pre-BEL.	7117B 04/27/87 ECD512A B78-1 G7 TiO2 pad in place prior to BEL; 1000Å Ti oxidized.	7120A 04/30/87 Th Oxide B67-2 G7110, Spin-on oxide/interlevel dielectric study;FES lifting @	7120B 04/30/87 Th Oxide B67-3 Spin-on oxide/interlevel dielectric study.	7120C 04/30/87 Th Oxide B67-4 Spin-on oxide/interlevel dielectric study.	7120D 04/30/87 Th Oxide B67-5 Spin-on oxide/interlevel dielectric study.	7121A 05/01/87 1000Å TiO2 B Buffer layer study;1x8/40/60,4	7121B 05/01/87 1000Å TO2 B79-2 Buffer layer study; blistered after sinter.	7121C 05/01/87 1000Å TiO2 B79-3 Buffer layer study; blistered after sinter.	7125A 05/05/87 ASM833 E	332	de cness	7125D 05/05/87 Nitride E 1/2 Std. FES thickness	7125E 05/05/87 Nitride E 1/2 Std. FES thickness	7125F 05/05/87 ECD512A E
BEL SOL-GEL ID, TYPE (Composition). & AGE		4/87 Nit+TiO2 T-2 G7110, (8/40/60,+10), 4 8cts @ rpm 750Å TiO2 under BEL study; 500Å Ti/1000Å Pt. Accuglass 305;3000rpm;2/ramp out @465°C/2 in O2;bottom half.	1/87 Nit+TiO2 T-3 G7110, (8/40/60,+10), 4 8cts @ rpm 1050Å TiO2 under BEL study; 500Å Ti/1000Å Pt. Accuglass 305;3000rpm;2/ramp out @465°C/2 in O2;bottom half	B78-4 G7110, (8/40/60,+10), 4 Pt.	B78-2 G7110, (8/40/60,+10), Pt.	B68-3 G7110, (8/40/60,+10), retric study.	B68-4 G7110, (8/40/60,+10), vctric study;FES lifting @ 7th ct.	B68-5 G7110, (8/40/60,+10), ctric study;FES lifting @ 5th ct	B77-5 G7110, (8/40/60,+10), wed pre-BEL.	B78-1 G7110, (8/40/60,+10), L; 1000Å TI oxidized	B67-2 G7110, (8/40/60,+10), 10 ctric study;FES litting @ 8th ct	B67-3 G7110, (8/40/60,+10), 10 etric study.	B67-4 G7110, (8/40/60,+10), 10 ctric study.	B67-5 G7110, (8/40/60,+10), 10 ctric study.	1/87 1000Å TiO2 B79-1 G7110/7072, Buffer layer study;1x8/40/60,+10:6x3/40/60,+10:1x8/40/60,+10.	B79-2 G7068/7022, after sinter.	B79-3 G7068/7020, after sinter.	B79-3 G7110, (8/40/60,+10),	B79-3 G7110, (8/40/60,+10), 15	B80-1 G7022, (0/50/50,+10), 103	B80-3 G7072, (3/40/60,+10),	B80-4 G7110, (8/40/60,+10), 15	B81-1 G7110, (8/40/60,+10), 15
. ID, COATS & SPIN AGE in days SPEED	0), 4 8cts @ rpm 000rpm;2/ramp out @465°C/2 in C	0), 4 8cts @ rpm 00rpm;2/ramp out @465°C/2 in (0), 4 8cts @ rpm 0000rpm;2/ramp out @465°C/2 in	0), 4 8cts @ rpm	o), 4 8cts @ rpm	0), 4 8cts @ rpm	0), 4 7cts @ rpm	0), 4 5cts @ rpm	0), 7 8cts @ rpm	0), 7 8cts @ rpm)), 10 8cts @ rpm)), 10 8cts @ rpm)), 10 8cts @ rpm)), 10 8cts @ rpm	1/6/1cts @ rpm	1/6/1cts @ rpm	1/6/1cts @ rpm)), 15 8cts @ rpm)), 15 8cts @ rpm), 103 4cts @ rpm)), 53 4cts @ rpm)), 15 4cts @ rpm)), 15 8cts @ rpm
t°C/%RH BAKE @ Spin PROFILE		2@400 02;bottom half.	2@400 O2;bottom half.	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400
SINTER	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	No Anneal	No Anneal	30@650inO2	30@650inO2	30@650inO2	30@650inO2
TEL TYPE	Fat1	Fat1	Fat1	Fat1	Fat1	Fat1	Fat1	Fat1	1001	512	Fat1	Fat1	Fat1	Fat1	Fat1	Fat1	Fat1	Fatt	Fat1	Fat1	Fatt	Fatt	512

SINTER TEL PROFILE TYPE	30@650InO2 Fat1	_	30@650inO2 NA	30@650inO2 LODM	30@650inO2 512	30@650inO2 512	30@650inO2 512	30@650InO2 NA	30@650inO2 NA	30@650inO2 NA	30@650inO2 512	30@650inO2 512	30@650inO2 NA	30@650inO2 NA	30@650inO2 NA		30@650inO2 NA	-						
N 1°C/%RH BAKE		2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400		2@400							
COATS & SPIN In days SPEED	8ds (22 8ds @ rpm	, 22 4cts @ rpm	25 8ds @ rpm	25 8cts @ rpm	25 8cts @ rpm	117. 8cts @ rpm	, 1 8cts @ rpm	i, 1 8cts @ rpm	1/7ds @ rpm	38 8cts @ rpm), 7 8cts @ rpm	1/7ds @ rpm	1/7ds @ rpm	1/7cts @ rpm		1/7cts @ rpm					1/7cts @ rpm 1/6/1cts @ rpm 1/6/1cts @ rpm 1@ 380°c. 10 380°c. 11 6cts @ rpm 1 @ 380°C. 2 8cts @ rpm 1 c. 2 8cts @ rpm 1 half at 750°C;alloy metal 10n	1/7cts @ rpm 1/6/1cts @ rpm (@ 380°c. 60 8cts @ rpm 11 6cts @ rpm 10 380°C. 42 6cts @ rpm °C. 8cts @ rpm half at 750°C;alloy metal 10n), 1 8cts @ rpm	1/7cts @ rpm 1/6/1cts @ rpm 1 (6) 380°c. 60 8cts @ rpm 1 (6) 380°c. 11 6cts @ rpm 1 (6) 380°C. 2 8cts @ rpm 2 8cts @ rpm 2 8cts @ rpm 1 (750°C;alloy metal 10n 1), 1 8cts @ rpm
SOL-GEL ID, (Composition), & AGE	/40,+10),	G7110, (8/40/60,+10), 22	G7110, (8/40/60<=10), 22	G7110, (8/40/60,+10), 25	G7110, (8/40/60,+10), 25	G7110, (8/40/60,+10), 25 5400°C.	G7022, (0/50/50,+10), 117	G7141, (0/50/50,+10),	G7141, (0/50/50,+10),	G7068/7141,	G7110, (8/40/60,+10), 38	G7141, (0/50/50,+10), 7	G6307/7141, gel	G7068/7141,	G6307/7141,	•	 G7068/7141, 	l G7068/7141, el G7110/7141, en 8/40/60. Metal alloyed 10min	i G7068/7141, el G7110/7141, on 8/40/60. Metal alloyed 10min G7092, (6/50/50,+10), on 8/40/60. Metal alloyed 10min	G7068/7141, al G7110/7141, G7110/7141, G7092, (6/50/50,+10), 60 G7092, (6/50/50,+10), 60 G7141, (0/50/50,+10), 11 G7141, (0/50/50,+10), 11 ore anneal. Metal alloyed 10min @ 380°C.	I	G7068/7141, al	i	i
SUBSTRATE BEL DESCRIPTION TYPE	1/87 Th Ox, TiO2 B79-4 Fatigue test of 3/60/40,+10.	2/87 Th Oxide B7?-? lon Gun Etch Studies.	2/87 Nit(35-) NA Spin-on TiO2 over nitride study	5/87 Th Oxide B56-4 lon Gun Etch Studies.	5/87 ECD512A B56-4 CMOS ECD512A	5/87 ECD512A B56-4 CMOS ECD512A;alloy Al for 10min@400°C.	9/87 ECD512A B56-4 CMOS ECD512A.	2/87 Nitride B56-4 Test new 0/50/50,+10.	2/87 Nitride B56-4 Test new 0/50/50,+10.	2/87 Si Wafer B56-4 For UNM optical measurements.	8/87 ECD512A B86 CMOS ECD512A with 8/40/60,+10.	8/87 ECD512A B86 CMOS ECD512A with 0/50/50,+10.	8/87 Th Oxide NA Buffer layer on SiO2;older 15/0/100 gel.	8/87 Th Oxide NA Buffer layer on SiO2;newer 15/0/100 gel.	Si Wafer NA	Buffer layer on Si;older 15/0/100 gel.	Buffer layer on Si;older 15/0/100 gel. 8/87 Si Wafer Buffer layer on Si;newer 15/0/100 gel.	Buffer layer on Si;older 15/0/100 gel 8/87 Si Wafer NA Buffer layer on Si;newer 15/0/100 gel 1/87 Th Ox,TiO2 B85-2 G7110/7141, Buffer layers;8/40/60 on 6x0/50/50 on 8/40/60. Metal alloyed 10min @ 380°c.	Buffer layer on Si;older 15/0/100 gel 8/87 Si Wafer NA G7068/7141, Buffer layer on Si;newer 15/0/100 gel 1/87 Th Ox,TIO2 B85-2 G7110/7141, Buffer layers;8/40/60 on 6x0/50/50 on 8/40/60. Metal alloyed 10min @ 380°c. 1/87 Th Ox,TIO2 B85-3 G7092, (6/50/50,+10), 60 Buffer layers;8/40/60 on 6x0/50/50 on 8/40/60. Metal alloyed 10min @ 380°c.	Buffer layer on Si;older 15/0/100 gel 8/87 Si Wafer NA Buffer layer on Si;newer 15/0/100 gel 1/87 Th Ox,TIO2 B85-2 Buffer layers;8/40/60 on 6x0/50/50 on 8/40/60. Metal is Th Ox,TIO2 B85-3 Buffer layers;8/40/60 on 6x0/50/50 on 8/40/60. Metal is Th Ox,TIO2 B85-3 1/87 Th Ox,TIO2 B85-4 G7141, (Film thinness study;etch top half before anneal. Metal	1ffer layer on Si;older 15/0/100 gel Si Wafer NA Iffer layer on Si;newer 15/0/100 ge NA Iffer layers;8/40/60 on 6x0/50/50 of NA Th Ox, TiO2 B85-3 Iffer layers;8/40/60 on 6x0/50/50 of NA Th Ox, TiO2 Th Ox, TiO3 Th O	Buffer layer on Si;older 15/0/100 gel 8/87 Si Wafer NA G7068/7141, Buffer layer on Si;newer 15/0/100 gel 1/87 Th Ox, TiO2 B85-2 G7092, (6/50/50,+10), 60 Buffer layers;8/40/60 on 6x0/50/50 on 8/40/60. Metal alloyed 10min @ 1/87 Th Ox, TiO2 B85-3 G7092, (6/50/50,+10), 60 Buffer layers;8/40/60 on 6x0/50/50 on 8/40/60. Metal alloyed 10min @ 1/87 Th Ox, TiO2 B85-4 G7141, (0/50/50,+10), 11 Film thinness study;etch top half before anneal. Metal alloyed 10min @ 380°C. 1/87 Th Ox, TiO2 B85-5 G7110, (8/40/60,+10), 42 Film thinness study;etch before anneal. Metal alloyed 10min @ 380°C. 1/87 Th Ox, TiO2 B79-5 G7153, (0/50/50,+0), 2 New composition;0/50/50,+0;anneal bottom half at 650 anneal top hal	Buffer layer on Si;older 15/0/100 gel. Si Wafer NA G7068/7141, 1/7cts @ rpm Buffer layer on Si;newer 15/0/100 gel. Buffer layer on Si;newer 15/0/100 gel. 1/87 Th Ox,TiO2 B85-2 G7110/7141, 1/6/1cts @ rpm Buffer layers;8/40/60 on 6x0/50/50 on 8/40/60. Metal alloyed 10min @ 380°c. 1/87 Th Ox,TiO2 B85-4 G7141, (0/50/50,+10), 11 6cts @ rpm Buffer layers;8/40/60 on 6x0/50/50 on 8/40/60. Metal alloyed 10min @ 380°c. 1/87 Th Ox,TiO2 B85-5 G7110, (8/40/60,+10), 42 6cts @ rpm Film thinness study;etch before anneal. Metal alloyed 10min @ 380°C. 4/87 Th Ox,TiO2 B79-5 G7153, (0/50/50,+0), 2 8cts @ rpm New composition;0/50/50,+0;anneal bottom half at 650,. anneal top half at 750°C;alloy metal 10min at 400°C. 4/87 Th Ox,TiO2 B82-1 G7154, (1/45/55,+10), 1 8cts @ rpm New Composition;1/45/55,+10. Metal alloyed 10min @ 380°C.	Buffer layer on Si;older 15/0/100 gel Si Wafer NA G7068/7141, Buffer layer on Si;newer 15/0/100 gel G7110/7141, Buffer layers;8/40/60 on 6x0/50/50 on 8/40/60. Metal alloyed 10min @ 1/87 Th Ox, TiO2 B85-3 G7092, (6/50/50,+10), 60 Buffer layers;8/40/60 on 6x0/50/50 on 8/40/60. Metal alloyed 10min @ 1/87 Th Ox, TiO2 B85-4 G7141, (0/50/50,+10), 11 Film thinness study;etch top half before anneal. Metal alloyed 10min @ 380°C. Film thinness study;etch before anneal. Metal alloyed 10min @ 380°C. H/87 Th Ox, TiO2 B79-5 G7153, (0/50/50,+0), 2 New composition;0/50/50,+0;anneal bottom half at 650. anneal top half New Composition;1/45/55,+10. Metal alloyed 10min @ 380°C. H/87 Th Ox, TiO2 B82-1 G7154, (1/45/55,+10), 1 New Composition;1/45/55,+10. Metal alloyed 10min @ 380°C.
FILM DATE	7131A 05/11/87 Fati	7132A 05/12/87	7132B 05/12/87 Spir	7135A 05/15/87	7135B 05/15/87 CMK	7135C 05/15/87 CM	7139A 05/19/87 CMK	7142A 05/22/87 Tes	7142B 05/22/87	7142C 05/22/87 For	7148A 05/28/87 CMK	7148B 05/28/87 CMK	7148C 05/28/87 Buff	7148D 05/28/87 Buff	7148E 05/28/87	;	05/2	0/90	06/0	7148F 05/28/87 Puff 7152A 06/01/87 7152B 06/01/87 7152C 06/01/87	0.50 0.60 0.60 0.60	0/90 0/90 0/90	0/90 0/90 0/90	0/90 0/90 0/90 0/90

															4								
TEL TYPE	512	512	512	512	512	512	512	512	Fat1	Fat1	Fat1	<u>1</u> 00	<u>Ю</u>	т Б	<u>б</u>	Fatt	Fat1	Fat1	Fat1	Fatt	Fat1	Fat1	Fat2
SINTER PROFILE	30@650InO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2
BAKE PROFILE	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400
t°C/%RH @ Spin											,												
COATS & SPIN S SPEED	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	. 8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	8ds @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm
SOL-GEL ID, (Composition), & AGE in days	G7141, (0/50/50,+10), 15	G7141, (0/50/50,+10), 15	9/87 ECD512A#13 B86-? G7141, (0/50/50,+10), 19 CMOS ECD512A with 0/50/50,+10;metal annealed 10min @ 400°C.	1/87 ECD512A#3 B91-? G7141, (0/50/50,+10), 21 CMOS ECD512A with 0/50/50,+10;10min @ 400°C metal anneal.	G7141, (0/50/50,+10), 21	1/87 ECD512A#20 B91-? G7141, (0/50/50,+10), 21 CMOS ECD512A with 0/50/50,+10;10min @ 400°C metal anneal	1/87 ECD512A#22 B91-? G7141, (0/50/50,+10), 21 CMOS ECD512A with 0/50/50,+10;metal annealed 10min @ 400°C.	G7141, (0/50/50,+10), 25 S rework of 7162B.	G7141, (0/50/50,+10), 25	G7141, (0/50/50,+10), 25	G7153, (0/50/50,+0), 13	G7141, (0/50/50,+10), 26	G7141, (0/50/50,+10), 26	G7141, (0/50/50,+10), 26	G7141, (0/50/50,+10), 26	G7141, (0/50/50,+10), 27 ling at 8th coat.	7/87 Th Ox, TiO2 B68-2 G7141, (0/50/50,+10), 27 Fatigue pattern for ILD study;wafer shattered on HP at 1st ct	G7141, (0/50/50,+10), 27	G7141, (0/50/50,+10), 27 sling at 8th coat.	G7141, (0/50/50,+10), 27	G7141, (0/50/50,+10), 27	G7141, (0/50/50,+10), 27	G7170, (0/50/50,+10), 3
SUBSTRATE BEL DESCRIPTION TYPE	5/87 ECD512A#7 B85-1 CMOS ECD512A with 0/50/50,+10.	5/87 ECD512A#9 B86-? CMOS ECD512A with 0/50/50,+10.	512A#13 B86-? 2A with 0/50/50,+10;me	ECD512A#3 B91-? D512A with 0/50/50,+10;10n	1/87 ECD512A#16 B91-? CMOS ECD512A with 0/50/50,+10.	ECD512A#20 B91-? D512A with 0/50/50,+10;10n	ECD512A#22 B91-? D512A with 0/50/50,+10;me	5/87 ECD512A#16 B91-? G7141, (0/ CMOS ECD512A with 0/50/50,+10;FES rework of 7162B.	Th Ox, TiO2 B82-3 t of 0/50/50,+10.	Th Ox, TiO2 B82-4 t of 0/50/50,+10.	Th Ox, TiO2 B82-5 t of 0/50/50,+0.	6/87 TDO1 B92-? Annealing test; TiN composition.	6/87 TDO1 B92-? Annealing test; TiN composition	6/87 TDO1 B92-? Annealing test; TiN composition	6/87 TDO1 B92-? Annealing test; TiN composition	7/87 Th Ox, TiO2 B68-1 G7141, Fatigue pattern for ILD study;FES peeling at 8th coat.	Dx,TiO2 B68-2 for ILD study;wafer sh	Dx,TIO2 B69-1 for ILD study.	7/87 Th Ox, TIO2 B69-2 G7141, Fatigue pattern for ILD study;FES peeling at 8th coat.	Th Ox, TiO2 B69-3 tern for ILD study.	Th Ox, TiO2 B69-4 tern for ILD study.	Th Ox, TiO2 B69-5 tern for ILD study.	Th Ox, TiO2 B87-1
DATE SUBS	06/05/87 ECD: CMOS ECD512	06/05/87 ECD: CMOS ECD512	06/09/87 ECD5 CMOS ECD512	06/11/87 ECD: CMOS ECD512	06/11/87 ECDE CMOS ECD512	06/11/87 ECDE CMOS ECD512	06/11/87 ECDE CMOS ECD512	06/15/87 ECDE CMOS ECD512	06/15/87 Th Ox, TiO2 Fatigue test of 0/50/50,+10	06/15/87 Th Ox, TiO2 Fatigue test of 0/50/50,+10	06/15/87 Th Ox, TiO2 Fatigue test of 0/50/50,+0.	06/16/87 Tile Annealing test;	06/16/87 TA Annealing test;	06/16/87 Ti Annealing test;	06/16/87 Ti Annealing test;	06/17/87 Th C Fatigue pattern	06/17/87 Th C Fatigue pattern	06/17/87 Th Ox, TiO2 E Fatigue pattern for ILD study.	06/17/87 Th C Fatigue pattern	06/17/87 Th Ox, TiO2 Fatigue pattern for ILD study.	06/17/87 Th Ox, TiO2 Fatigue pattern for ILD study.	06/17/87 Th Ox,TiO2 Pratigue pattern for ILD study.	06/22/87 Th C ILD study
	7156A	7156B	7160A	7162A	7162B	7162C	7162D	7166A	7166B	7166C	7166D	7167A	7167B	7167C	7167D	7168A	7168B	7168C	7168D	7168E	7168F	7168G	7173A

FILM	DATE	SUBSTRATE DESCRIPTION	BEL TYPE	SOL-GEL ID, (Composition), & AGE in o	COATS & SPIN days SPEED	t°C/%RH @ Spin	BAKE PROFILE	SINTER PROFILE	TEL
7173B	06/22/87 ILD study.	Th Ox, TiO2 dy.	B87-2	50/50,+10), 3	8cts (2@400	30@650inO2	Fat2
7173C	06/22/87 ILD study.	Th Ox,TIO2 dy.	B87-3	G7170, (0/50/50,+10), 3	8cts @ rpm		2@400	30@650inO2	Fat2
7173D	06/22/87 ILD study.	Th Ox, TiO2 dy	B87-4	G7170, (0/50/50,+10), 3	8cts @ rpm		2@400	30@650inO2	Fat2
7173E	06/22/87 ILD study.	Th Ox,TIO2 dy	B87-5	G7170, (0/50/50,+10), 3	8ds @ rpm		2@400	30@650inO2	Fat2
7173F	06/22/87 ILD study.	Th Ox,TiO2 dy	B88-1	G7170, (0/50/50,+10), 3	8cts @ rpm		2@400	30@650inO2	Fat2
7173G	. 06/22/87 ILD study.	Th Ox, TIO2 dy	B88-2	G7170, (0/50/50,+10), 3	8cts @ rpm		2@400	30@650inO2	Fat2
7173H	06/22/87	Th Ox, TIO2	B88-3	G7170, (0/50/50,+10), 3	8cts @ rpm		2@400	30@650inO2	Fat2
71731	06/22/87 ILD study.	Th Ox,TiO2 dy	B88-4	G7170, (0/50/50,+10), 3	8cts @ rpm		2@400	30@650inO2	Fat2
7173J	06/22/87	Th Ox, TiO2	B88-5	G7170, (0/50/50,+10), 3	8cts @ rpm		2@400	30@650inO2	Fat2
7173K	06/22/87 Etch test.	Th Ox, TiO2 st	B78-3	G7170, (0/50/50,+10), 3	8cts @ rpm		2@400	30@650inO2	₹
7175A	06/24/87 CMOS I	ECD512A#5 ECD512A with 0/50/	96or97 /50,+10;alloy r	4/87 ECD512A#5 96or97 G7170, (0/50/50,+10), 5 CMOS ECD512A with 0/50/50,+10;alloy metal 10min at 400°C.	8cts @ rpm		2@400	30@650inO2	512
7175B	06/24/87 CMOS I	ECD512A#10 ECD512A with 0/50/	96or97 /50,+10;alloy r	4/87 ECD512A#10 96or97 G7170, (0/50/50,+10), 5 CMOS ECD512A with 0/50/50,+10;alloy metal 10min at 400°C.	8cts @ rpm		2@400	30@650inO2	512
71750	06/24/87 CMOS I	ECD512A#24 ECD512A with 0/50	96or97 /50,+10;alloy	4/87 ECD512A#24 96or97 G7170, (0/50/50,+10), 5 8cts @ rpm CMOS ECD512A with 0/50/50,+10;alloy metal 10min at 400°C. Wafer broken during processing, 1/2+ remaining.	8cts @ rpm oken during processing, 1.	/2+ remaining.	2@400	30@650inO2	512
7175D	06/24/87 ILD study.	Th Ox,TIO2 dy	B89-1	G7153, (0/50/50,+0), 22	8cts @ rpm		2@400	30@650inO2	Fat2
7175E	06/24/87	Th Ox, TiO2	B89-2	G7153, (0/50/50,+0), 22	8cts @ rpm		2@400	30@650inO2	Fat2
7175F	06/24/87 Shatter	4/87 Th Ox, TIO2 B89- Shattered during 1st coat bake	B89-3 pake	G7153, (0/50/50,+0), 22	8cts @ rpm		2@400	30@650inO2	Fat2
7175G	06/24/87 ILD study.	Th Ox,TIO2 dy	B89-4	G7153, (0/50/50,+0), 22	8 cts @ rpm		2@400	30@650inO2	Fat2
7175H	06/24/87 Accugla	Th Ox,TIO2	B90-5 nd 10th coats;	4/87 Th Ox,TiO2 B90-5 G7170, (0/50/50,+10), 5 10*cts @ rpm 2@400 Accuglass Ti-900 as 1st and 10th coats;3000rpm, std FES bake. Alternate electrode screening;occasional wide spaced cracks.	10*cts @ rpm ate electrode screening;o	ccasional wide s	2@400 paced cracks.	30@650inO2	LODM
7177A	06/26/87 CMOS	6/87 ECD512A#12 96or97 CMOS ECD512A with 0/50/50,+10.	96or97 /50,+10	G7170, (0/50/50,+10), 7	8cts @ rpm		2@400	30@650inO2	512
7183A	07/02/87 ILD study.	Orb512TW dy	~	G7170, (0/50/50,+10), 13	8cts @ rpm		2@400	30@650inO2	512
7183B	07/02/87 ILD study.	Orb512TW	~	G7170, (0/50/50,+10), 13	8cts @ rpm		2@400	30@650inO2	512
7183C	07/02/87 ILD study.	Orb512TW idy.	٠	G7170, (0/50/50,+10), 13	8cts @ rpm		2@400	30@650inO2	512
7183D	07/02/87 ILD study.	Orb512TW Idy.	٠	G7170, (0/50/50,+10), 13	8cts @ rpm		2@400	30@650inO2	512

FILM	DATE	SUBSTRATE DESCRIPTION	BEL I TYPE	SOL-GEL ID, (Composition), & AGE in days	COATS & SPIN ys SPEED	t°C/%RH BAKE @ Spin PROFILE	SINTER PROFILE	TEL TYPE
7187A	07/06/87 CMOS	04m129#6 ECD512A with 0/5	? 0/50,+10;alloy	6/87 04m129#6 ? G7170, (0/50/50,+10), 17 CMOS ECD512A with 0/50/50,+10;alloy metal 10min at 400°C.	8cts @ rpm	2@400	30@650inO2	512
7187B	07/06/87 CMOS	04m129#14 ECD512A with 0/5	? 0/50,+10;alloy	6/87 04m129#14 ? G7170, (0/50/50,+10), 17 CMOS ECD512A with 0/50/50,+10;alloy metal 10min at 400°C.	8cts @ rpm	2@400	30@650inO2	512
7187C	07/06/87 CMOS	04m129#15 ECD512A with 0/5	? :0/50,+10;alloy	6/87 04m129#15 ? G7170, (0/50/50,+10), 17 CMOS ECD512A with 0/50/50,+10;alloy metal 10min at 400°C.	8cts @ rpm	2@400	30@650inO2	512
7187D	07/06/87 CMOS	04m129#17 ECD512A with 0/5	م 0/50,+10;alloy	6/87 04m129#17 ? G7170, (0/50/50,+10), 17 CMOS ECD512A with 0/50/50,+10;alloy metal 10min at 400°C.	8cts @ rpm	2@400	30@650inO2	512
7187E	07/06/87 CMOS	04m129#21 ECD512A with 0/5	? :0/50,+10;alloy	6/87 04m129#21 ? G7170, (0/50/50,+10), 17 CMOS ECD512A with 0/50/50,+10;alloy metal 10min at 400°C.	8cts @ rpm	2@400	30@650inO2	512
7190A	07/09/87 CMOS	06m061#1 ECD512A with 0/5	B100-1 0/50,+10;alloy	9/87 06m061#1 B100-1 G7170, (0/50/50,+10), 20 CMOS ECD512A with 0/50/50,+10;alloy metal 10min at 400°C. Reworked from BEL	8cts @ rpm om BEL.	2@400	30@650inO2	512
7190B	07/09/87 CMOS	06m061#9 ECD512A with 0/5	B100-2 0/50,+10;alloy	9/87 06m061#9 B100-2 G7170, (0/50/50,+10), 20 CMOS ECD512A with 0/50/50,+10;alloy metal 10min at 400°C. Reworked from BEI	8cts @ rpm om BEL.	2@400	30@650inO2	512
7190C	07/09/87 FES et	9/87 7 FES etch studies, 0/50/50,+10.	B53-2 0,+10.	G7170, (0/50/50,+10), 20	8cts @ rpm	2@400	30@650inO2	512
7203A	07/22/87 1st BEI	2/87 Unifilm#1 L	Uf#1 tterer.	G7194, (0/50/50,+10), 9	8cts @ rpm	2@400	30@650inO2	Fat2
7204A	07/23/87 Semi-A	3/87 Th Oxide NA Semi-Auto sol-gel dispense with EFD system.	NA Se with EFD s	G7170, (0/50/50,+10), 34 ystem.	8cts @ rpm	2@400	¥	ş
7204B	07/23/87 ILD study.	Th Ox,TiO2 ldy.	102-1	G7194, (0/50/50,+10), 10	8cts @ rpm	2@400	30@650InO2	ş
7204C	07/23/87 ILD study.	Th Ox,TIO2	102-2	G7194, (0/50/50,+10), 10	8cts @ rpm	2@400	30@650inO2	¥
7204D	07/23/87 ILD study.	Th Ox,TIO2	102-3	G7194, (0/50/50,+10), 10	8cts @ rpm	2@400	30@650inO2	ş
7204E	07/23/87 ILD study.	Th Ox,TIO2 udy	102-4	G7194, (0/50/50,+10), 10	8cts @ rpm	2@400	30@650inO2	ş
7204F	07/23/87 ILD study.	Th Ox,TiO2 udy	102-5	G7194, (0/50/50,+10), 10	8cts @ rpm	2@400	30@650inO2	ş
7205A	07/24/87 CMOS	06m061#2 ECD512A with 0/5	BM103 50/50,+10;alloy	4/87 06m061#2 BM103 G7194, (0/50/50,+10), 11 8cts @ rpm 2@400 CMOS ECD512A with 0/50/50,+10;alloy metal 10min at 400°C. 1st sinter reached 610°C only; 2nd sinter, 30min@650°C.	8cts @ rpm ached 610°C only; 2nd :	2@400 sinter, 30min@650°C.	30@650inO2	512
7205B	07/24/87 CMOS	06m061#5 ECD512A with 0/5	BM103 50/50,+10;alloy	4/87 06m061#5 BM103 G7194, (0/50/50,+10), 11 8cts @ rpm 2@400 CMOS ECD512A with 0/50/50,+10;alloy metal 10min at 400°C. 1st sinter reached 610°C only; 2nd sinter, 30min@650°C.	8cts @ rpm ached 610°C only; 2nd	2@400 sinter, 30min@650°C.	30@650inO2	512
7205C	07/24/87 CMOS	4/87 06m061#11 BM103 G7194, CMOS ECD512A with 0/50/50,+10;alloy metal 10min	BM103 50/50,+10;alloy	G7194, (0/50/50,+10), 11 y metal 10min at 400°C. 1st sinter re	8cts @ rpm ached 610°C only; 2nd	, (0/50/50,+10), 11 8cts @ rpm 2@400 at 400°C. 1st sinter reached 610°C only; 2nd sinter, 30min@650°C.	30@650inO2	512
7205D	07/24/87 CMOS	4/87 06m061#20 BM103 G7194, CMOS ECD512A with 0/50/50,+10;alloy metal 10min	BM103 50/50,+10;alloy	G7194, (0/50/50,+10), 11 y metal 10min at 400°C. 1st sinter re	8cts @ rpm ached 610°C only; 2nd	, (0/50/50,+10), 11 8cts @ rpm at 400°C. 1st sinter reached 610°C only; 2nd sinter, 30min@650°C.	30@650inO2	512
7205E	07/24/87 CMOS	4/87 06m061#25 BM103 G7194, CMOS ECD512A with 0/50/50,+10;alloy metal 10min	BM103 50/50,+10;alloy	G7194, (0/50/50,+10), 11 y metal 10min at 400°C. 1st sinter re	8cts @ rpm ached 610°C only; 2nd	, (0/50/50,+10), 11 8cts @ rpm at 400°C. 1st sinter reached 610°C only; 2nd sinter, 30min@650°C.	30@650inO2	512
7209A	07/28/87 ILD study.	م ybr	٠	G7194, (0/50/50,+10), 15	8ds @ rpm	2@400	30@650inO2	Fat2
7209B	07/28/87 ILD study.	ر ، ypr	٠	G7194, (0/50/50,+10), 15	8cts @ rpm	2@400	30@650inO2	Fat2
7209C	07/28/87 ILD study.	, , , , , , , , , , , , , , , , , , ,	٠	G7194, (0/50/50,+10), 15	8ძა @ rpm	2@400	30@650inO2	Fat2

FILM	DATE	SUBSTRATE DESCRIPTION	BEL TYPE	SOL-GEL ID, (Composition), & AGE in days	COATS & SPIN SPEED	t•C/%RH @ Spin	BAKE PROFILE	SINTER PROFILE	TEL TYPE
7209D	07/28/87 ILD study.	ر . ybr	۰	G7194, (0/50/50,+10), 15	8cts @ rpm		2@400	30@650inO2	Fat2
7209E	07/28/87 ILD study.	Th Ox, TiO2	104-1	G7194, (0/50/50,+10), 15	8cts @ rpm		2@400	30@650inO2	Fat2
7209F	07/28/87 ILD study.	Th Ox, TiO2	104-2	G7194, (0/50/50,+10), 15	8cts @ rpm		2@400	30@650inO2	Fat2
7209G	07/28/87 ILD study.	Th Ox, TiO2	104-3	G7194, (0/50/50,+10), 15	8cts @ rpm		2@400	30@650inO2	Fat2
7209H	07/28/87 ILD study.	Th Ox, TIO2	104-4	G7194, (0/50/50,+10), 15	8cts @ rpm		2@400	30@650inO2	Fat2
72091	07/28/87 ILD study.	Th Ox, TiO2 Jdy.	104-5	G7194, (0/50/50,+10), 15	8cts @ rpm		2@400	30@650inO2	Fat2
7211A	07/30/87 CMOS	06m061#3t ECD512A with 0/50/5	104-5 50,+10;allo	0/87 06m061#3t 104-5 G7194, (0/50/50,+10), 16 CMOS ECD512A with 0/50/50,+10;alloy metal 10min at 400°C. Top half of wafer	8cts @ rpm		2@400	30@650inO2	512
7211B	07/30/87 CMOS	06m061#7 ECD512A with 0/50/9	104-5 50,+10;allo	0/87 06m061#7 104-5 G7194, (0/50/50,+10), 16 CMOS ECD512A with 0/50/50,+10;alloy metal 10min at 400°C	8cts @ rpm		2@400	30@650inO2	512
7211C	07/30/87 CMOS	06m061#18 ECD512A with 0/50/9	104-5 50,+10;allo	0/87 06m061#18 104-5 G7194, (0/50/50,+10), 16 CMOS ECD512A with 0/50/50,+10,alloy metal 10min at 400°C	8cts @ rpm		2@400	30@650inO2	512
7211D	07/30/87 CMOS	06m061#22 ECD512A with 0/50/9	104-5 50,+10;allo	0/87 06m061#22 104-5 G7194, (0/50/50,+10), 16 CMOS ECD512A with 0/50/50,+10,alloy metal 10min at 400°C.	8cts @ rpm		2@400	30@650inO2	512
7211E	07/30/87 Failure	06m061#3b analysis;cracking/fur	Gone rrowing arc	0/87 06m061#3b Gone G7194, (0/50/50,+10), 16 Failure analysis;cracking/furrowing around TiO2. Bottom half of wafer.	8cts @ rpm		2@400	30@650inO2	512
7212A	07/31/87 #1;140	1/87 06m079#2 N #1;1400Å Ti(normal Ti,1000Å)	¥ . (¥	G7194, (0/50/50,+10), 17	8cts @ rpm		2@375	30@650inO2	512
7212B	07/31/87 #2;100	1/87 06m079#21 #2;1000Å Ti(normal Ti,1000Å).	¥ Æ	G7194, (0/50/50,+10), 17	8cts @ rpm		2@375	30@650inO2	512
7212C	07/31/87 #4;500	1/87 06m079#11 #4;500Å TI(normal Ti,1000Å).	¥ .	G7194, (0/50/50,+10), 17	8cts @ rpm		2@375	30@650inO2	512
7212D	07/31/87 #3;100	1/87 08m079#19 #3;1000Å Ti(normal Ti,1000Å).	¥ . . ₹	G7194, (0/50/50,+10), 17	8cts @ rpm		2@425	30@650inO2	512
7212E	07/31/87 #5;500	1/87 06m079#16 #5;500Å TI(normal TI,1000Å)	¥ .	G7194, (0/50/50,+10), 17	8cts @ rpm		2@425	30@650inO2	512
7218A	08/06/87 UNM o	6/87 1x1/16quartz UNM optical studies	₹	G7194, (0/50/50,+10), 24	8cts @ rpm		2@400	30@650inO2	₹
7218B	08/06/87 UNM o	6/87 1x1/16quartz UNM optical studies	₹	G7068/7194,	1/7cts @ rpm		2@400	30@650inO2	¥
7218C	08/06/87 UNM o	6/87 1x1/16quartz UNM optical studies	≨	G7068, (15/0/100,+10), 150	8cts @ rpm		2@400	30@650inO2	ş
7218D	08/06/87 85HB5	6/87 Th Ох, TiO2 85HB5;TIP-7;#01.	~	G7194, (0/50/50,+10), 24	8cts @ rpm		2@400	30@650inO2	Fat2
7218E	08/06/87 P42;85	6/87 Th Ox,TiO2 P42;85HB5;Ti-10;#02.	~	G7194, (0/50/50,+10), 24	8cts @ rpm		2@400	30@650inO2	Fat2
7218F	08/06/87 P32;84	6/87 Th Ox, TiO2 P32;84HB9;Ti-8;#03	~	G7194, (0/50/50,+10), 24	8cts @ rpm		2@400	30@650inO2	Fat2
7218G	08/06/87 83HB9	6/87 Th Ox, TiO2 83HB9;TiP-5;#04.	~	G7194, (0/50/50,+10), 24	8cts @ rpm		2@400	30@650inO2	Fat2

half cleared.		•	,		
TI/PT/TI	G7194, (0/50/50,+10), 28	8cts @ rpm	2@400	30@650inO2	Fat2
TI/PT/TI	G7194, (0/50/50,+10), 28	8cts @ rpm	2@400	30@650inO2	Fat2
TIVPT/TI	G7194, (0/50/50,+10), 28	8cts @ rpm	2@400	30@650inO2	Fat2
INPTAIL	G7194, (0/50/50,+10), 28	8ძა @ rpm	2@400	30@650inO2	Fat2
11-1 paked/sintered in new	11-1 G7225, (0/50/50,+10), 9 8cts @ rpm paked/sintered in new facility. G7225 first sol-gel made in new facility on new apparatus.	8αs @ rpm new facility on new apparatus.	2@400	30@650inO2	Fat2
11-2 baked/sintered in new	11-2 G7225, (0/50/50,+10), 9 8cts @ rpm baked/sintered in new facility. G7225 first sol-gel made in new facility on new apparatus.	8cts @ rpm n new facility on new apparatus.	2@400	30@650inO2	Fat2
t 11-3 baked/sintered in new	11-3 G7225, (0/50/50,+10), 9 8cts @ rpm baked/sintered in new facility. G7225 first sol-gel made in new facility on new apparatus.	8cts @ rpm ก new facility on new apparatus.	2@400	30@650inO2	Fat2
11-4 G7225, (0/50/ 0aked/sintered in new facility. G7225	G7225, (0/50/50,+10), 9 facility. G7225 first sol-gel made in	50,+10), 9 8cts @ rpm first sol-gel made in new facility on new apparatus.	2@400	30@650inO2	Fat2
11-5 G7225, (0/50/ Daked/sintered in new facility. G7225	G7225, (0/50/50,+10), 9 facility. G7225 first sol-gel made in	50,+10), 9 8cts @ rpm first sol-gel made in new facility on new apparatus.	2@400	30@650inO2	Fat2
14-1 o; FES coat/bake/sinte	G7225, (0/50/50,+10), 11 or in new facility. G7225 first sol-ge	24-1 G7225, (0/50/50,+10), 11 8cts @ rpm 3; FES coat/bake/sinter in new facility. G7225 first sol-gel made in new facility on new apparatus.	2@400 lus.	30@650inO2	Fat2
G7225, (0/50/9); FES coat/bake/sinter in new facility.	G7225, (0/50/50,+10), 11 or in new facility. G7225 first sol-ge	2)+10), 11 8cts @ rpm G7225 first sol-gel made in new facility on new apparatus.	2@400 tus.	30@650inO2	Fat2
		22Feb91 reprint of FES coating log (last modified Wed, Nov 4, 1987 4:11pm. Page 24	g (last modified \	Wed, Nov 4, 1987 4:11	pm. Page 24

FILM	DATE	SUBSTRATE DESCRIPTION	BEL TYPE	SOL-GEL ID, (Composition), & AGE in days	COATS & SPIN t°C/%RH ys SPEED @ Spin	H BAKE	SINTER PROFILE	TEL
7218H	08/06/87 P22;85	6/87 Th Ox, TIO2 P22;85HB10;TI-6;#05.	٤	G7194, (0/50/50,+10), 24	8ძა @ rpm	2@400	30@650inO2	Fat2
72181	08/06/87 P21;84	6/87 Th Ox, TiO2 P21;84HB10;Ti-5;#06.	~	G7194, (0/50/50,+10), 24	8cts @ rpm	2@400	30@650inO2	Fat2
7218J	08/06/87 P41;83	6/87 Th Ox, TiO2 P41;83B4;Ti-9;#07.	<i>~</i>	G7194, (0/50/50,+10), 24	8cts @ rpm	2@400	30@650inO2	Fat2
7222A	08/10/87 Titaniu	0/87 06m061 Titanium over BEL	TI/PT/TI	G7194, (0/50/50,+10), 28	8cts @ rpm	2@400	30@650inO2	512
7222B	08/10/87 Titaniu	0/87 06m061#13 Titanium over BEL	TI/PT/TI	G7194, (0/50/50,+10), 28	8cts @ rpm	2@400	30@650InO2	512
7222C	08/10/87 Titaniu	0/87 06m061#14 Titanium over BEL.	TI/PT/TI	G7194, (0/50/50,+10), 28	8cts @ rpm	2@400	30@650InO2	512
7222D	08/10/87 Titaniu	0/87 06m061#17 Titanium over BEL	TI/PT/TI	G7194, (0/50/50,+10), 28	8ds @ rpm	2@400	30@650inO2	512
7222E	08/10/87 Titaniu	0/87 06m061#1? Titanium over BEL	TI/PT/TI	G7194, (0/50/50,+10), 28	8ds @ rpm	2@400	30@650inO2	512
7222F	08/10/87 Stande	0/87 06m061#4 Standard BEL	STD BEL	G7194, (0/50/50,+10), 28	8cts @ rpm	2@400	30@650inO2	512
7222G	08/10/87 Standa	0/87 06m061#10 Standard BEL	STD BEL	G7194, (0/50/50,+10), 28	8cts @ rpm	2@400	30@650inO2	512
7222H	08/10/87 Standa	0/87 06m061#8 Standard BEL	STD BEL	G7194, (0/50/50,+10), 28	8cts @ rpm	2@400	30@650inO2	512
72221	08/10/87 Titaniu	0/87 Th Ox, TiO2 TI/PT/T Titanium over BEL, top half cleared.	TI/PT/TI	G7194, (0/50/50,+10), 28	8ds @ rpm	2@400	30@650inO2	Fat2
7222J	08/10/87 Titaniu	0/87 Th Ox, TIO2 Trtanium over BEL.	TI/PT/TI	G7194, (0/50/50,+10), 28	8cts @ rpm	2@400	30@650inO2	Fat2
7222K	08/10/87 Titaniu	0/87 Th Ox, TiO2 Titanium over BEL.	TI/PT/TI	G7194, (0/50/50,+10), 28	8cts @ rpm	2@400	30@650inO2	Fat2
7222L	08/10/87 Titaniu	0/87 Th Ox, TiO2 Titanium over BEL	TI/PT/TI	G7194, (0/50/50,+10), 28	8cts @ rpm	2@400	30@650inO2	Fat2
7222M	08/10/87 Titaniu	0/87 Th Ox, TiO2 Titanium over BEL.	TI/PT/TI	G7194, (0/50/50,+10), 28	8cts @ rpm	2@400	30@650inO2	Fat2
7234A	08/22/87 Std.BE	2/87 Th Ox,TIO2 11-1 G7229 Std.BEL; FES coated/baked/sintered in new facility.	11-1 ad/sintered ir		i, (0/50/50,+10), 9 8cts @ rpm G7225 first sol-gel made in new facility on new apparatus.	2@400 is.	30@650inO2	Fat2
7234B	08/22/87 Std.BE	2/87 Th Ox, TiO2 11-2 G7225 Std.BEL; FES coated/baked/sintered in new facility.	11-2 ed/sintered ir		i, (0/50/50,+10), 9 8cts @ rpm G7225 first sol-gel made in new facility on new apparatus.	2@400 Is.	30@650inO2	Fat2
7234C	08/22/87 Std.BE	2/87 Th Ox,TiO2 11-3 G7228 Std.BEL; FES coated/baked/sintered in new facility.	11-3 ed/sintered ir		i, (0/50/50,+10), 9 8cts @ rpm G7225 first sol-gel made in new facility on new apparatus.	2@400 is.	30@650inO2	Fat2
7234D	08/22/87 Std.BE	2/87 Th Ox,TIO2 11-4 G722/ Std.BEL; FES coated/baked/sintered in new facility.	11-4 ed/sintered in	u)	i, (0/50/50,+10), 9 8cts @ rpm G7225 first sol-gel made in new facility on new apparatus.	2@400 Is.	30@650inO2	Fat2
7234E	08/22/87 Std.BE	2/87 Th Ox,TIO2 11-5 G722 Std.BEL; FES coated/baked/sintered in new facility.	11-5 ed/sintered in	G7225, (0/50/50,+10), 9 in new facility. G7225 first sol-gel ma	i, (0/50/50,+10), 9 8cts @ rpm G7225 first sol-gel made in new facility on new apparatus.	2@400 Is.	30@650inO2	Fat2
7236A	08/24/87 Std.BE	Th Ox, TiO2 EL w/500Å Ti cap; FE	14-1 ES coat/bak	4/87 Th Ox,TiO2 14-1 G7225, (0/50/50,+10), 11 8cts @ rpm Std.BEL w/500Å Ti cap; FES coat/bake/sinter in new facility. G7225 first sol-gel made in new facility on new apparatus.	8cts @ rpm ol-gel made in new facility on new a	2@400 apparatus.	30@650inO2	Fat2
7236B	08/24/87 Std.BE	Th Ox,TIO2 EL w/500Å Ti cap; Fł	14-2 ES coat/bak	4/87 Th Ox, TiO2 14-2 G7225, (0/50/50,+10), 11 8cts @ rpm Std.BEL w/500A Ti cap; FES coat/bake/sinter in new facility. G7225 first sol-gel made in new facility on new apparatus.	8cts @ rpm ol-gel made in new facility on new	2@400 apparatus.	30@650inO2	Fat2

TEL TYPE	Fat2	Fat2	٠	٠	٠	٠	٠	~	٠	٠	٠	٢	۷	٠	٠	~	~	~	~	Fat2	Fat2	Fat2	Fat
SINTER PROFILE	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@GEOinOo
BAKE PROFILE	2@400 ratus.	2@400 ratus.	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	00400
t°C/%RH @ Spln	ty on new appa	ty on new appa																					
COATS & SPIN SPEED	8cts @ rpm jel made in new facili	8cts @ rpm jel made in new facili	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	0.40
SOL-GEL ID, (Composition), & AGE in days	4/87 Th Ox, TiO2 15-1 G7225, (0/50/50,+10), 11 8cts @ rpm 2/ Std. BEL w/500Å Ti cap; FES coat/bake/sinter in new facility. G7225 first sol-gel made in new facility on new apparatus.	4/87 Th Ox, TiO2 15-2 G7225, (0/50/50,+10), 11 8cts @ rpm Std. BEL w/500Å Ti cap; FES coat/bake/sinter in new facility. G7225 first sol-gel made in new facility on new apparatus.	G7194, (0/50/50,+10), 45 M O2	7/87 Th Ox, TiO2 74-1 G7194, (0/50/50,+10), 45 Coated/Baked at UNM; Sintered at Krysalis, 5 LPM O2.	G7225, (0/50/50,+10), 14 M O2	7/87 Th Ox, TiO2 74-1 G7225, (0/50/50,+10), 14 Coated/Baked at UNM; Sintered at Krysalis, 5 LPM O2.	7/87 Th Ox, TiO2 90-1 G7194, (0/50/50,+10), 45 Coated/Baked at Krysalis; Sintered at UNM, 2 LPM O2.	G7194, (0/50/50,+10), 45 LPM O2	7/87 Th Ox, TiO2 90-1 G7225, (0/50/50,+10), 14 Coated/Baked at Krysalis; Sintered at UNM, 2 LPM O2.	G7225, (0/50/50,+10), 14 LPM O2	G7194, (0/50/50,+10), 45 M O2	G7194, (0/50/50,+10), 45	G7225, (0/50/50,+10), 14 M O2	G7225, (0/50/50,+10), 14	G7225, (0/50/50,+10), 15 LPM O2	90-3 G7243, (0/50/50,+10), <1 at Krysalis, 5 LPM O2;80°F,35%RH.	1/87 Th Ox,TiO2 90-3 G7243, (0/50/50,+10), 1 Coated/Baked/Sintered at Krysalis, 5 LPM O2;74-78°F.	1/87 Th Ox, TiO2 90-4 G7243, (0/50/50,+10), 1 Coated/Baked/Sintered at Krysalis, 5 LPM O2;81°F,65%RH?.	2/87 Th Ox,TiO2 90-4 G7243, (0/50/50,+10), 2 Coated/Baked/Sintered at Krysalis, 5 LPM O2;65°F,68%RH.	G7243, (0/50/50,+10), 4	G7243, (0/50/50,+10), 4	G7243, (0/50/50,+10), 4	
BEL I TYPE	15-1 ES coat/ba	15-2 ES coat/bal	74-1 UNM, 2 LP	74-1 intered at Kr	74-1 UNM, 2 LP	74-1 intered at Kr	90-1 Sintered at	90-1 t Krysalis, 5	90-1 Sintered at	90-1 t Krysalis, 5	90-2 UNM, 2 LP	90-2	90-2 UNM, 2 LP	90-2	90-3 t Krysalis, 5	90-3 t Krysalis, 5	90-3 t Krysalis, 5	90-4 t Krysalis, 5	90-4 t Krysalis, 5	18-1 °C. %RH.	≃	≃	۲
SUBSTRATE DESCRIPTION	Th Ox, TiO2 . w/500Å Ti cap; F	Th Ox, TIO2 . w/500Å Ti cap; F	7/87 Th Ox, TiO2 74-1 Coated/Baked/Sintered at UNM, 2 LPM O2.	Th Ox, TiO2 Baked at UNM; Si	7/87 Th Ox, TiO2 74-1 Coated/Baked/Sintered at UNM, 2 LPM O2.	Th Ox, TiO2 Baked at UNM; Si	Th Ox, TiO2 Baked at Krysalis	7/87 Th Ox, TiO2 90-1 G Coated/Baked/Sintered at Krysalis, 5 LPM O2.	Th Ox, TiO2 Baked at Krysalis	7/87 Th Ox,TiO2 90-1 G Coated/Baked/Sintered at Krysalis, 5 LPM O2.	7/87 Th Ox, TiO2 90-2 Coated/Baked/Sintered at UNM, 2 LPM O2.	7/87 Th Ox, TiO2 Coated/Baked at UNM.	7/87 Th Ox,TiO2 90-2 Coated/Baked/Sintered at UNM, 2 LPM O2.	7/87 Th Ox, TiO2 Coated/Baked at UNM.	8/87 Th Ox,TiO2 90-3 Coated/Baked/Sintered at Krysalis, 5 LPM O2.	1/87 Th Ox, TiO2 Coated/Baked/Sintered a	Th Ox, TiO2 'Baked/Sintered a	Th Ox, TiO2 /Baked/Sintered a	Th Ox, TIO2 Baked/Sintered a	4/87 Th Ox, TIO2 Coated in chem lab:	2	2	2
DATE COATED	08/24/87 Std.BEL	08/24/87 Std.BEL	08/27/87 Coated//	08/27/87 Coated/	08/27/87 Coated//	08/27/87 Coated/	08/27/87 Coated/	08/27/87 Coated/	08/27/87 Coated/	08/27/87 Coated/	08/27/87 Coated/	08/27/87 Coated/	08/27/87 Coated/	08/27/87 Coated/	08/28/87 Coated/	08/31/87 Coated/	09/01/87 Coated/	09/01/87 Coated/	09/02/87 Coated/	09/04/87 Coated	09/04/87 Coated	09/04/87 Coated	79/70/00
FILM	7236C	7236D	7239A	7239B	7239C	7239D	7239E	7239F	7239G	7239H	72391	7239J	7239K	7239L	7240A	7243A	7244A	7244B	7245A	7247A	7247B	7247C	7247

FILM	DATE COATED	SUBSTRATE DESCRIPTION	BEL TYPE (SOL-GEL ID, (Composition), & AGE	in days	COATS & SPIN SPEED	t°C/%RH @ Spin	BAKE PROFILE	SINTER PROFILE	TEL
7247E	09/04/87 Coated	4/87 Th Ox, TiO2 Coated in chem lab; °C,	18-5 %RH	G7243, (0/50/50,+10), 4		8cts @ rpm		2@400	30@650inO2	Fat2
7247F	09/04/87 Coated	4/87 Th Ox, TiO2 Coated in chem lab; °C,	16	-1 G7243, (0/50/50,+10), 4 8cts @ rpm %RH;500Å Ti cap over BEL. Anna's 1st FES coats - cts 2 thru 5.	a's 1st FES coats	8cts @ rpm is - cts 2 thru 5.		2@400	30@650inO2	Fat2
7247G	09/04/87 Coated	4/87 Th Ox,TIO2 Coated in chem lab; °C,	16	-2 G7243, (0/50/50,+10), 4 8cts @ rpm %RH;500Å Ti cap over BEL. Anna's 1st FES coats - cts 2 thru 5.	1), 4 a's 1st FES coats	8cts @ rpm ts - cts 2 thru 5.		2@400	30@650inO2	Fat2
7247H	09/04/87 Coated	2	16	16-3 G7243, (0/50/50,+10), 4 8cts @ rpm ——%RH;500Å Ti cap over BEL. Anna's 1st FES coats - cts 2 thru 5.	a's 1st FES coats	8cts @ rpm s - cts 2 thru 5.		2@400	30@650InO2	Fat2
72471	09/04/87 Coated	4/87 Th Ox, TiO2 Coated in chem lab;°C,		16-4 G7243, (0/50/50,+10), 4 8cts @ rpm	1), 4 a's 1st FES coat	8cts @ rpm s - cts 2 thru 5.		2@400	30@650inO2	Fat2
7247J	09/04/87 Coated	4/87 Th Ox,TiO2 Coated in chem lab; °C,		16-5 G7243, (0/50/50,+10), 4 8cts @ rpm ——%RH;500Å Ti cap over BEL. Anna's 1st FES coats - cts 2 thru 5.	1), 4 a's 1st FES coats	8cts @ rpm s - cts 2 thru 5.		2@400	30@650inO2	Fat2
7248A	09/05/87 Coated	5/87 Th Ox, TiO2 Coated in chem lab; °C,		-1 G7243, (0/50/50,+10), 5 %RH;400Å Ti cap over BEL.), 5	8cts @ rpm		2@400	30@650inO2	Fat2
7248B	09/05/87 Coated	5/87 Th Ox, TiO2 Coated in chem lab; °C,		17-2 G7243, (0/50/50,+10), 5 —%RH;400Å Ti cap over BEL.		8cts @ rpm		2@400	30@650inO2	Fat2
7248C	09/05/87 Coated	5/87 Th Ox, TiO2 Coated in chem lab;°C.	1	-3 G7243, (0/50/50,+10), 5 %RH;400Å Ti cap over BEL.		8cts @ rpm		2@400	30@650inO2	Fat2
7248D	09/05/87 Coated	5/87 Th Ox, TiO2 Coated in chem lab; °C,	17	17-4 G7243, (0/50/50,+10), 5 —%RH;400Å Ti cap over BEL		8cts @ rpm		2@400	30@650inO2	Fat2
7248E	09/05/87 Coated	5/87 Th Ox, TiO2 Coated in chem lab;C,		17-5 G7243, (0/50/50,+10), 5 ——%RH;400Å Ti cap over BEL.		8cts @ rpm		2@400	30@650inO2	Fat2
7251A	09/08/87 Coated	8/87 06M061-1 ? G7243, Coated in chem lab;77°F,42%RH;500Å Ti cap over BEI	7 %RH;500Å Ti	G7243, (0/50/50,+10), 8 cap over BEL		8cts @ rpm		2@400	30@650inO2	512
7251B	09/08/87 Coated	8/87 06M061-2 ? G7243, Coated in chem lab;77°F,42%RH;500Å Ti cap over BEI	? %RH;500Å Ti o	G7243, (0/50/50,+10), 8 cap over BEL		8cts @ rpm		2@400	30@650inO2	512
7251C	09/08/87 Coated	8/87 06M061-7 ? G7243, Coated in chem lab;77°F,42%RH;500Å Ti cap over BEI	? %RH;500Å Ti	G7243, (0/50/50,+10), 8 cap over BEL.		8cts @ rpm		2@400	30@650inO2	512
7251D	09/08/87 Coated	8/87 06M061-11 ? G7243, Coated in chem lab;77°F,42%RH;500Å Ti cap over BEL	? %RH;500Å Ti	G7243, (0/50/50,+10), 8 cap over BEL.		8cts @ rpm		2@400	30@650inO2	512
7253A	09/10/87 Wafers	0/87 Nitride#11 NONE Wafers for National Semiconductor.	NONE nductor.	G7243, (0/50/50,+10), 10		8cts @ rpm		2@400	Ą	ž
7253B	09/10/87 Wafers	0/87 Oxide#23 NONE Wafers for National Semiconductor.	NONE nductor.	G7243, (0/50/50,+10), 10		8cts @ rpm		2@400	¥	¥
7253C	09/10/87 Wafers	0/87 Nitride#2 YES Wafers for National Semiconductor.	YES nductor	G7243, (0/50/50,+10), 10		8cts @ rpm		2@400	30@650inO2	¥
7253D	09/10/87 Wafers	0/87 Oxide#13 YES Wafers for National Semiconductor	YES nductor	G7243, (0/50/50,+10), 10		8cts @ rpm		2@400	30@650inO2	¥
7253E	09/10/87 500Å T	0/87 06M061-13 500Å Ti cap over BEL	٠	G7243, (0/50/50,+10), 10		8cts @ rpm		2@400	30@650inO2	512
7253F	09/10/87 500Å T	0/87 06M061-14 500Å Ti cap over BEL	٠	G7243, (0/50/50,+10), 10		8cts @ rpm		2@400	30@650inO2	512
7253G	09/10/87 500Å T	0/87 06M061-17 500Å Ti cap over BEL	<i>-</i>	G7243, (0/50/50,+10), 10		8cts @ rpm		2@400	30@650inO2	512
7253H	09/10/87 500Å T	0/87 06M061-20 500A Ti cap over BEL	٠	G7243, (0/50/50,+10), 10	`	8cts @ rpm		2@400	30@650inO2	512

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TEL	512	Ą	¥.	Fat2	Fat2	Fat2	Fat2	Fat2	Fat2	Fat2	Fat2	Fat2	Fat2	Fat2	Fat2	Fat2	ž	¥.	₹	Fat2	Fat2	Fat2	Fat2	•
SINTER PROFILE	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	30@650inO2	
BAKE PROFILE	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	2@400	
t°C/%RH @ Spln																								
COATS & SPIN SPEED	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	8cts @ rpm	5cts @ 2000rpm	5cts @ 2000rpm	5cts @ 2000rpm	5cts @ 3000rpm	5cts @ 4000rpm	8cts @ 2000rpm	4cts @ 3000грm	
SOL-GEL ID, (Composition), & AGE in days	0/50,+10),	G7243, (0/50/50,+10), 11 solvent ore-wash	G7243, (0/50/50,+10), 11	G7243, (0/50/50,+10), 11	G7243, (0/50/50,+10), 11	G7243, (0/50/50,+10), 11	G7243, (0/50/50,+10), 11	G7243, (0/50/50,+10), 11	G7243, (0/50/50,+10), 15	G7243, (0/50/50,+10), 15	G7243, (0/50/50,+10), 15	G7243, (0/50/50,+10), 15	G7243, (0/50/50,+10), 15	G7243, (0/50/50,+10), 15	G7243, (0/50/50,+10), 15	G7243, (0/50/50,+10), 15	G7259, (0/50/50,+10), 6 μπ,sint μπ	GI7264A, (0/50/50,+10), 1 um,sint um	9	A GI	G7264, (0/50/50,+10), 4 A,post sint A.	G7259, (0/50/50,+10), 13	G7264, (0/50/50,+10), 8	
BEL TYPE	2	NONE	NONE	CB8295	CB8296	CB8297	CB8298	CB8299	F002-6 cold/cold/cold.	F002-10 cold/hot/cold.	F002-13 Mot/cold	F002-16 Vcold/cold.	F002-2 cold/cold/cold.	F002-8 Id/hot/cold.	F002-11 Uhot/cold.	F002-15 Vcold/cold.				post bake	post bake		0.5M gel.	
SUBSTRATE DESCRIPTION	06M061-21	1/87 Nitride NONE G7243, (0/5 Wafers for National Semiconductor:no solvent ore-wash.	1/87 Oxide NONE G7243, (0/8) Wafers for National Semiconductoring solvent pre-wash	Th Ox, TiO2	Th Ox, T102	Th Ox, T102	Th Ox, T102	Th Ox, T102	· · 5/87 Th Ox,TIO2 Ti/Pt/Ti 850/1200/250Å ∞l	5/87 Th Ox, TIO2 Ti/Pt/Ti 850/1200/250Å ∞l	5/87 Th Ox, TIO2 F002-13 TI/Pt/Ti 850/1200/250Å hot/hot/cold.	5/87 Th Ox, TIO2 F002-16 TI/Pt/TI 850/1200/250Å hot/cold/cold.	5/87 Th Ox, TiO2 Ti/Pt/Ti 850/1200/250Å ∞l	5/87 Th Ox, TiO2 F002-8 Ti/Pt/Ti 850/1200/250Å cold/hot/cold	5/87 Th Ox, TiO2 F002-11 Ti/Pt/Ti 850/1200/250Å hot/hot/cold.	5/87 Th Ox, TiO2 F002-15 Ti/Pt/Ti 850/1200/250Å hot/cold/cold.	2/87 Th Ox, TiO2 Coating thickness trials:bake	2/87 Th Ox, TiO2 Coating thickness trials:bake	2/87 Th Ox, TiO2 Coating thickness trials:bake	5/87 Th Ox,TIO2 Thickness/etch rate study;post bake	5/87 Th Ox,TIO2 Thickness/etch rate study;post bake	9/87 Th Ox, TIO2	9/87 Th Ox, TIO2 Illinois gel study - Krysalis 0.5M gel.	
DATE COATED D	ಫ	09/11/87 Wafers fo	09/11/87 Wafers fo	09/11/87	. : 09/11/87	09/11/87	09/11/87	09/11/87	 09/15/87 Ti/Pt/Ti 8	09/15/87 Ti/Pt/Ti 8	09/15/87 Ti/Pt/Ti 8	09/15/87 Ti/Pt/Ti 8	09/15/87 Ti/Pt/Ti 6	09/15/87 Ti/Pt/Ti 8	09/15/87 Ti/Pt/Ti 8	09/15/87 Ti/Pt/Ti 8	09/22/87 Coating	09/22/87 Coating	09/22/87 Coating	09/25/87 Thicknes	09/25/87 Thickne	09/29/87 Illinois a	09/29/87 Illinois g	

7258G

7258H

7265A

7265B

7265C

7258F

72531

7254F

7254G

7258A

7258B

7258C

7258D

7258E

7254C

7254B

7254A

7254D

7254E

7272B

7272A

7268B

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ш	30@650inO2
BAKE	2@400
t°C/%RH @ Spin	
COATS & SPIN t°C/%RH SPEED @ Spin	5cts @ 4000rpm
SOL-GEL ID, (Composition), & AGE in days	GI7264B, (0/50/50,+10), 8,1 basic.
BEL TYPE	hydrolyzed
SUBSTRATE DESCRIPTION	19/87 Th Ox, TiO2 Thois gel study - 4mol/mol hydrolyzed basic
FILM DATE ID COATED (7272C 09/29/87
FILM	7272C

Ephilitis

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FAILURE ANALYSIS REPORT

SUBJECT: SEM and Optical Microscopic study of selected low failure rate die on Wafer #7148A

DATE: June 16, 1987

BY: Leo Chapin

Following is preliminary data on failure analysis of wafer#7148A. Dave Eaton provided us with a bit failure map of 6 selected die having relatively low, random (but repeatable) bit failures. Two of six die were examined and photographed using the Hitachi 450 SEM at UNM. All six die were examined using the Nikon Optiphot in differential interference contrast (Nomarski) mode at X1000 magnification.

at X1000	o magnificati	on.
DIE# F	AILED BIT	DESCRIPTION OF FAILURE
0,+7	44,7	Missing TEL on bottom cell
	57,6	Blister on bottom cell
0,+4	4,7*	TEL filament bridge with 5,7
SEM	5,7*	(see above)
photos	17,1*	Blister on cell
·	23,1*	Small blisters on cell
	48,5*	Blister (adjacent cell,49,5, also blistered)
	56,6*	? (adjacent good cell,57,6, blistered)
+2,+1	8,1*	? nothing apparent
SEM	56,4 *	Missing FES in capacitors
photos	56,5 *	N N N N
	57,4 *	a a a
	57,5*	" " " NOTE: Some adjacent cells which tested good also had FES missing from capacitors.*
	63,7*	Blister 25 missing it on capacital 3.
+5,+3	51,0	Small blister on top cell
	53,7	Blister on bottom cell
	60,0	Blister on top cell
+5,+2	25,1	Blister on top cell
	31,1	Very small blisters(5) on top cell
	32,2	? (blister on 33,2)
	48,7	Blister on bottom cell
	49,7	Medium blisters(2) on bottom cell
	51,1	Blister on bottom cell
	52,7	Blister on bottom cell
	63,3	Blister on bottom cell; 6+small to v.small blisters on top cell

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-2,-1	36,1	V.small blister (large blister on 37,2)
	49,0*	Blister on cell
	50,6*	? nothing apparent
	54,5*	Blister on cell
	55,4*	Blister on cell
	56,7*	? nothing apparent

The blisters on failed bits, except where noted, had a diameter that was typically 2/3 to 3/4 the width of BEL. On die#+2,+1 a fast (and somewhat subjective) survey was made of blister size. The blisters were catagorized as + (larger than), = (same size), and - (smaller than) relative to the typical failed bit blister. Of the 1024 capacitors viewed, one had a blister in the + (larger than) catagory, 21 had blisters in the = (same size) catagory, and 209 had blisters in the - (smaller than) catagory (this last catagory is the most subjective since cells with few very small blisters were not counted).

The asterisk following the FAILED BIT address indicates that SEM and/or optical microscope photos were made. In addition to these photos the following were made:

+2,+1	9,2	Good bit with large (= same as) blister but partly off BEL
	8,2b	Metal over TEL for comparison with 8,1 (? nothing apparent but bad)
	22,5t	"Good bit" with missing TE1 over top cell
-2,-1	-,-	Typical area
=2,-3	-,-	Typical area

All photos related to failure analysis are kept in a binder (titled "Failure Analysis Reports") with a copy of the report.

Efforts are underway to catagorize blister size (and other defects) more objectively.

Some 7148A film data:

FES COATING LOG Krysalis Confidential

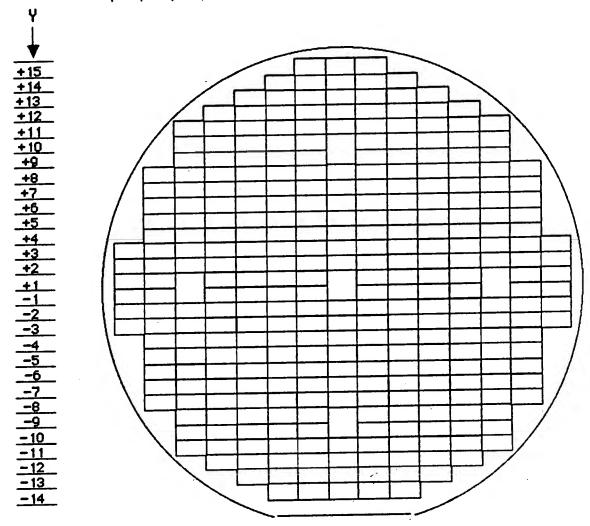
FILM ID SUBSTRATE BEL TEL BAKE ANNEAL DAY MADE

7148A ...ECD512A ...B86 ...512 ...2@400 ...30@650in02 05/28/87 67110(8/40/60,+10);8cts;38 days old NOTES:CMOS ECD512A with 8/40/60,+10

Attached is the wafer die addressing scheme used in this report (comments solicited and accepted, perhaps).

16JUN87:LNC

ECD512A Die Address Guide (X,Y)



16JUN87:LHC